CFP MSA Management Interface Specification

100/40 Gigabit Transceiver Package Multi-Source Agreement

Version 2.2 r06a

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1 REVISION HISTORY

Revision	Date	Objective	By
External NDA Draft 0.1	12/23/2008	Initial release, work in progress	Jiashu Chen
External NDA Draft 0.2	01/26/2009	2nd release for review	Jiashu Chen
External NDA Draft 0.3	02/19/2009	3rd release for review	Jiashu Chen
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External NDA Draft 0.4F	04/07/2009	Error corrected version of 0.4E for review	Jiashu Chen
Publication Draft 1.0	04/13/2009	First full draft for releasing to public.	Jiashu Chen
External NDA Draft 1.1	6/22/2009	Pre Public release Draft 1.2	Jiashu Chen
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External NDA Draft 1.3R5	4/16/2010	Pre Public Release for Draft 1.4	Jiashu Chen
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Publication Version 1.4 (r2)	6/4/2010	Pre Publication release	Jiashu Chen
Publication Version 1.4 (r3)	6/15/2010	Pre Publication release for MSA Members	Jiashu Chen
Publication Version 1.4 (r4)	6/21/2010	Pre Publication release	Jiashu Chen
Publication Version 1.4 (r5)	6/22/2010	Publication release	Jiashu Chen
Draft Version 2.0 (r7)	6/30/2011	Pre Publication release for public review. This release implements OIF MSA-100G DWDM Transmission Module Management Interface Requirements. Specifically, added new Section 6: MSA-100GLH Module Management Interface, which includes: - Module Base and Extended ID Information; - Module Command, Control & FAWS; - MDIO Write Flow Control - Additional Monitored Parameters and Performance Monitoring Functions for Long Haul DWDM; - Software Upgrade Capability; - Auxiliary Channel Interface over MDIO; - Generic Data Upload Capability - Bulk Data Transfer Procedure. Added new Section 1.3: CFP MIS Version Compatibility. This release also includes CFP MIS V1.4 updates: - Sec. 4.10.2/Table 11: Note 2 is amended "Further commands should NOT be issued without returning to idle"; - Sec. 5.1/Table 18: 0x8007h, code point 09h = P1I1-3D1 (NRZ 40G 1300nm, 10km) - Sec. 5.1/Table 18: 0x8071h.b2 & b1 changed to indicate whether Amplitude Adjustment Function is supported in A280h~A28Fh. - Sec. 5.5/Table 22: A011h: Initial value changed to 1b=1/64 Tx Ref Clk Rate Select; - Sec. 5.5/Table 22: A012h: Initial value changed to 1b=1/64 Rx Ref Clk Rate Select; - Sec. 5.5/Table 22: A029h: Initial value changed to A7F8h - Sec. 5.6/Table 23: A250h Initial value changed to E0DCh. See complete list of changes in file: Comment_Log_CFP-MSA-MIS_V2p0_02_0312.xlsx	J. Anderson
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Version 2.2r01	9/18/2012	CFP MSA MIS 2.2 is released to support CFP2 and CFP2 applications, as well as enhancing all the contents from Version 2.0. Version 2.2(r1) is released for review, representing work in	Jiashu Chen

		progress. Not final.	
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REFERENCES

1. IEEE Standard 802.3-2012
2. IEEE Std. 802.3ba™-2010 (Obsolete, replaced by IEEE Standard 802.3-2012)
3. INF-8074i, XENPAK MSA Issue 3.0
4. INF-8077i, XFP Specification Rev. 4.5 (Not directly referenced)
5. CFP MSA Hardware Specification Draft 1.4
6. OIF-MSA-100GLH-EM-01.1, September, 2011
7. CFP MSA CFP2 HW Spec Rev02

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1 DOCUMENT SUMMARY

1.1 Background

This technical document, CFP MSA Management Interface Specification, has been created by the CFP MSA group as a basis for a technical agreement between CFP module users and vendors, together with its companion document *CFP MSA Hardware Specification*.

This document is not a warranted document. Each CFP or MSA-100GLH module supplier will have their own datasheet. If the users wish to find a warranted document, they should consult the datasheet of the chosen module vendor.

The CFP MSA group reserves the rights at any time to add, amend, or withdraw technical data contained in this document.

1.2 CFP Management Interface

CFP MSA Hardware Specification specifies the use of Management Data Input/Output (MDIO) as the management interface between a Host and a CFP module. While the hardware specification defines the hardware aspects of the MDIO interface such as its electrical characteristics and timing requirements, this document defines a set of MDIO registers suitable for CFP or MSA-100GLH module applications following MDIO interface definition in IEEE 802.3 Clause 45.

1.3 CFP Management Interface Specification Version Compatibility

Version 1.4 (r5) is the first public publication release of the CFP Management Interface Specification supporting the CFP MSA Hardware Specification V1.4.

Version 2.0 (r9) of the CFP Management Interface Specification is extended to support the OIF MSA-100GLH module electro-mechanical specification [6]. In particular, Section 6 is added in Version 2.0 which specifies added functionality and registers for supporting the OIF MSA-100GLH module management interface. Implementation of B000h page registers specified in Section 6 requires the use of Write Flow Control which is inherently incompatible with register write access implemented in Version 1.4.

To provide version backwards compatibility, A000h page registers specified in Version 1.4 are maintained in Version 2.0 without requiring Write Flow Control. The Version 2.0 A000h page registers are not extended or modified for supporting the OIF MSA-100GLH module management interface. There are some modifications to the Version 2.0 A000h page registers to correct errors in Version 1.4 A000h page registers.

To provide version forward compatibility, Version 1.4 A000h page registers are duplicated in the B000h page registers of Version 2.0 with enhancements and modifications for supporting the OIF MSA-100GLH module management interface. The B000h page registers requires Write Flow Control. In this manner, host system and module suppliers may implement Version 2.0 B000h page registers for supporting both CFP MSA and OIF MSA-100GLH hardware specifications. A host system implementing Version 1.4 CFP MSA Management Interface Specification would not be compatible with modules implementing Version 2.0 CFP MSA Management Interface Specification.

Version 2.2 (r04) is the 3rd public publication release with the enhancement to support CFP2 and CFP4 modules, in particular the CFP MSA CFP2 Hardware Specification (Currently in Draft Revision 0.2). Majority of the changes are implemented in Sections from 1 to 5. Whenever it is applicable Section 6 is modified for consistency.

For the convenience of reference, new register names introduced in the subsequent releases are marked with version number such as [2.2] to indicate that this register is introduced in version 2.2 release. Similar approach has been applied to registers that were introduced in version 2.0.

1.4 Content of this document

Section 1 is the summary of this document. Section 2 provides an overview of the CFP management interface, including a sample block diagram, MDIO command frame, and the CFP register set. Section 3 layouts the overview of the CFP register set. Section 4 presents detailed discussions of the Host/Module control and signaling theory. Section 5 gives a series of tables describing the details of all CFP registers. Section 6 specifies management interface functions and registers for supporting the OIF MSA-100GLH DWDM Transmission Module.

1.5 Notations

1.5.1 Hardware Signal Name

Signals transmitted over CFP or MSA-100GLH module connector pins are considered as hardware signals. Hardware signals names are directly quoted from the CFP MSA Hardware Specification or MSA-100GLH, formed with all upper case letters and numbers with the exception of a lower case letter as the post script for some cases. Examples are MOD_LOPWR and MOD_RSTn.

1.5.2 Soft (MDIO) Signal Name

Signals transmitted over CFP Management Interface are considered as "Soft" signals or MDIO signals. They are represented by CFP Registers or register bits. Soft signals have their names denoted by one or more words or acronyms connected with or without underscores. If the name consists of multiple words each word shall have its first character capitalized. Examples are Soft GLB_ALRM Test, Soft Module Reset, etc. Some Soft signals used as the defaults for programmable hardware pins are denoted in the manner of Hardware Signal names, such as GLB_ALRM, HIPWR_ON, and MOD_READY.

1.5.3 CFP Register Name and Address

The names of CFP registers are formed with one or more English words, with each word's first character capitalized and space in between. Each register address is a 16-bit hex number. When a particular bit in a register is addressed its address is denoted by x.y where the x is the register address and y is the bit address, a decimal number ranging from 0 to 15. When several bits in a register are addressed the address format is x.y~z, where y and z are boundary bits. The sign "~" is used to represent all the bits in between.

1.5.4 Numbers

Hex numbers are post-fixed by a lower case letter "h", for example, A000h. Binary numbers are post-fixed by a lower case letter "b" such as 11b and 1101b. Decimal numbers have neither prefix nor postfix. With this notation, an example of bit 15 at register A001 (hex) has the format of A001h.15.

1.5.5 Special Characters

Whenever possible, the special characters are avoided. For example, the symbol of micrometer is designated as "um" or micro-meter instead of "μm" to prevent format loss in the editing process.

1.6 Glossary

The often used nomenclatures in this document are listed in the following glossary table for reference.

Table 1 Glossary

Terminology	Description
APD	Avalanche Photodiode
BOL	Beginning Of Life
IEEE 802.3	IEEE Standard 802.3-2012
CFP MSA Specifications	CFP MSA Specifications define a hot-pluggable optical transceiver form factor to enable 40Gbps and 100Gbps applications, including next-generation High Speed Ethernet (40GbE and 100GbE). CFP MSA Specifications consist of two major documents: CFP MSA Hardware Specification and CFP MSA Management Interface Specification (this document).
CFP module	A transceiver compliant to CFP MSA. The term "module" refers to CFP module unless otherwise specified.
CFP register(s)	A CFP register collects certain related management information in a basic form of a 16-bit word, occupying one MDIO register address. The term "register" refers to CFP register unless otherwise specified.
CMU	Clock Multiplier Circuit.
Control	It refers to the Host control functions to the module over Management Interface. It also includes the support of programmable control pin logic.
DDM	Digital Diagnostic Monitoring. It includes CFP module functions of A/D value reporting, FAWS logic, and programmable alarm pin logic.

Terminology	Description
FAWS	Fault, Alarm, Warning, and Status.
GLB_ALRM	It is a CFP module internally generated signal that drives GLB_ALRMn pin.
GLB_ALRMn	Global alarm hardware signal pin defined in CFP MSA Hardware Specification.
HIPWR_ON	High power mode of module operation.
Host	It is equivalent to Station Management Entity (STA) of IEEE 802.3, Reference 1. It sources MDC (MDIO Clock).
Host Lane	It refers to high speed data lane between a Host and a CFP module.
HW_Interlock	It is a logic signal CFP module generates internally based on Hardware Interlock (Reference 5). It is defined as follows: 1 if CFP module power dissipation/consumption is greater than the Host cooling capacity 0 if CFP module power dissipation/consumption is equal or less than the Host cooling capacity or if Hardware Interlock is not used.
MOD_LOPWR	Hardware signal driving CFP module into Low-Power State. Reference 5 CFP MSA Hardware Specification Rev. 1.4 for details.
MOD_LOPWRs	Combined Module Low Power Signal. Refer to Section 4.1.1.2.
MOD_RSTn	Hardware signal driving CFP module into Reset State. See Reference 5 CFP MSA Hardware Specification Rev. 1.4 for details.
MOD_RSTs	Combined Module Reset Signal. Refer to Section 4.1.1.1.
MSA-100GLH	OIF 100G Long-Haul DWDM Transmission Module Electro-mechanical MSA
Network Lane	It refers to data lane between CFP module and network, say, optical network.
NVM	Non-Volatile Memory
NVR	Non-Volatile Register
OMA	Optical Modulation Amplitude
PLL	Phase-Locked Loop
PMD	Physical Medium Dependent
Signal	Information represented by hardware pins or CFP register bits and/or transmitted over the management interface or hardware connector.
SOA	Solid-State Optical Amplifier
TX_DIS	Refer to Reference 5 for description.
TX_DISs	Combined Transmitter Disable Signal. Refer to Section 4.1.1.3.
User	The customer of CFP module.
Vendor	The manufacturer of CFP module.
VR	Volatile Register

1

2 CFP MANAGEMENT INTERFACE

2.1 Overview

CFP Management Interface is the main communication interface between a Host and a CFP module. Host uses this interface to control and monitor the startup, shutdown, and normal operation of the CFP modules it manages. This interface operates over a set of hardware pins through the CFP module connector and a set of software based protocols.

The primary protocol of CFP Management Interface is specified using MDIO bus structure following the general specification of IEEE 802.3 Clause 45 and on-going IEEE 802.3 40GbE and 100GbE standardization project.

From a hardware point of view, CFP Management Interface consists of following 8 hardware signals: 2 hardware signals of MDC and MDIO, 5 hardware signals of Port Address, and 1 hardware signal GLB_ALRMn.

MDC is the MDIO Clock line driven by the Host and MDIO is the bi-directional data line driven by both the Host and module depending upon the data directions. The CFP Management Interface uses these hardware signals in the electrical connector to instantiate the MDIO interface, listed in Table 2.4 MDIO Interface Pins, in *CFP MSA Hardware Specification*.

From a software/protocol point of view, CFP Management Interface consists of the MDIO management frame, a set of CFP registers, and a set of rules for host control, module initialization, and signal exchange between these two. To avoid the conflict with IEEE 802.3, CFP register set does not use the addresses from 0000h to 7FFFh at the present time. The CFP registers use the addresses from 8000h to FFFFh, totaling 32768 addresses.

2.1.1 CFP/CFP2/CFP4 Port Address Compatibility

Compared with 5 hardware port address pins for CFP modules, both CFP2 and CFP4 support only 3 hardware MDIO Port Address pins (Reference 7) which result in a reduced directing space from 32 to 8. For multi device type applications where a mix of port address modes (32 and 8 addresses) is expected, the user shall need to correctly select the right module type to avoid a potential address conflict. MSA specifies the following mechanism to support the compatibility.

2.1.1.1 CFP/CFP2/CFP4 Common Functionality

The two Port Address most significant bits (MSBs) are **ignored** by the CFP2 and CFP4 module. Hence the effective port address range of CFP2 and CFP4 modules is from 0 (00000b) to 31 (11111b), with the module responding to four port addresses in the address range. Host hardware decoding of two MSBs is required to select the correct CFP2 or CFP4 module.

2.1.1.2 CFP2 Only Multi-device Type Functionality

The CFP2 module only responds if the two Port Address MSBs are zero. Hence the effective port address range of this CFP2 module is from 0 (00000b) to 7 (00111b). This enables assigning of the non-zero values of the two MSBs to other device types on a common MDIO bus with CFP2 modules.

2.1.1.3 Configuration of Port Address Support

An NVR register bit (807Eh.5) is used to indicate what MDIO port address scheme is used for a module. See register description for details. For all new modules, CFP/CFP2/CFP4 Common MDIO Port Address Scheme is recommended by MSA.

2.2 Specifications

With compliance to IEEE 802.3 Clause 45, CFP MSA defines the following additional specifications for CFP MDIO interface.

a) Support of MDC rate up to 4 MHz while maintaining the downward compatibility to 100 kHz.
b) Both read and write activities occurring on the rising edge of the MDC clock only.
c) Supports MDIO Device Address 1 only, among 32 available addresses.

2.2.1 Optional Features

This specification provides a number of optional features. Compliance with this specification does not require the implementation of these optional features by the module supplier. All such optional features shall be clearly identified as "Optional" in the corresponding register and bit definitions as well as the related text.

2.2.1.1 Optional Controls

The module supplier shall explicitly indicate the presence (or absence) of each optional control in the Module Enhanced Options registers in NVR register space. This allows the host to dynamically determine feature availability on a module-by-module basis.

2.2.1.2 Optional FAWS signals

Optional FAWS register bits do not require identification in Module Enhanced Options registers in NVR register space.

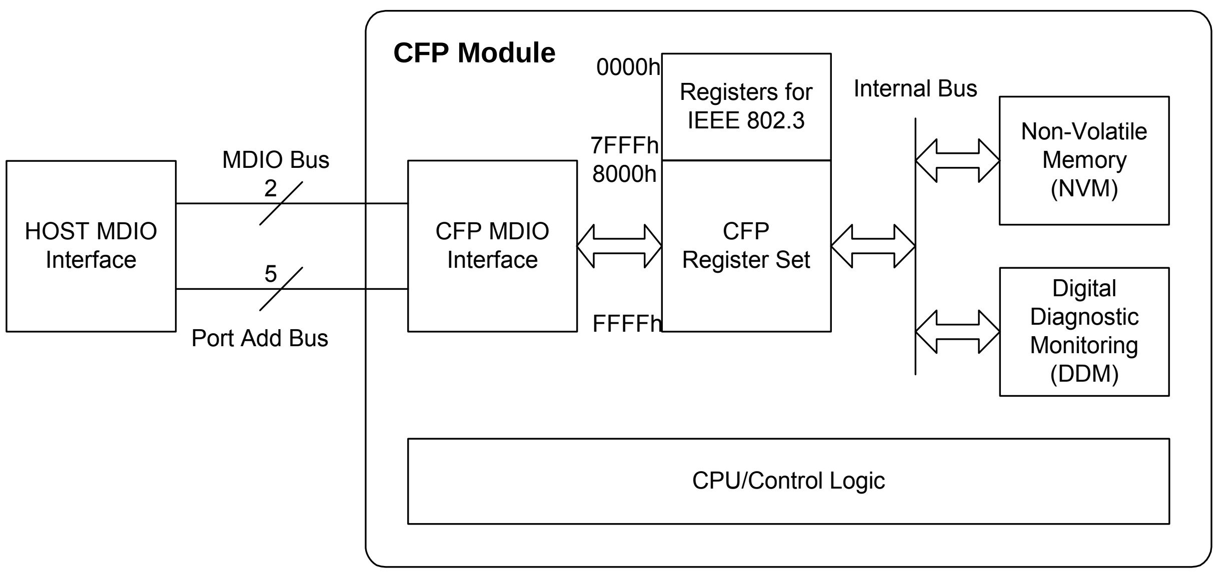
2.3 Interface Architecture

CFP MSA exemplifies a MDIO interface architecture illustrated in *Figure 1 CFP Management Interface Architecture*. This architecture recommends a dedicated MDIO logic block in the CFP module to handle the high rate MDIO data and a CFP register set that is divided into two register groups, the Non-Volatile Registers (NVR) and the Volatile Registers (VR). The NVRs are connected to a Non-Volatile Memory device for ID/Configuration data storage. Over the internal bus system, the VRs are connected to a device that executes the Host control commands and reports various Digital Diagnostic Monitoring (DDM) data. Note in the rest of this documentation, independent of implementation, CFP registers are also referred as NVRs or VRs.

In implementation, CFP registers shall use fast memory to shadow the NVM data and the DDM data. The shadow registers decouple the Host-side timing requirements from module vendor's internal processing, timing, and hardware control circuit introduced latency. Then this CFP shadow register set shall meet the following requirements:

a) It supports dual access from the Host and from module internal operations such as NVM and DDM data transfers.
b) It supports continuous Host access (read and write) with fast access memory at maximum MDC rate of 4 MHz.
c) It allows the uploading of NVM content into the CFP register shadow during module initialization. The data saving from CFP register shadow to NVM shall also be supported.
d) It supports the DDM data update periodically during the whole operation of the module. The maximum data refresh period shall meet the 100 ms for single network lane applications. If the number of lanes is greater than one, then the maximum data refresh period shall be 50 * (N + 1) ms, where N = number of network lanes supported in the application.
e) It supports the whole CFP register set including all NVRs and VRs.
f) Incomplete or otherwise corrupted MDIO bus transactions shall be purged from memory and disregarded.
g) The port address shall be allowed to change in fly without a module reset.

Figure 1 CFP Management Interface Architecture

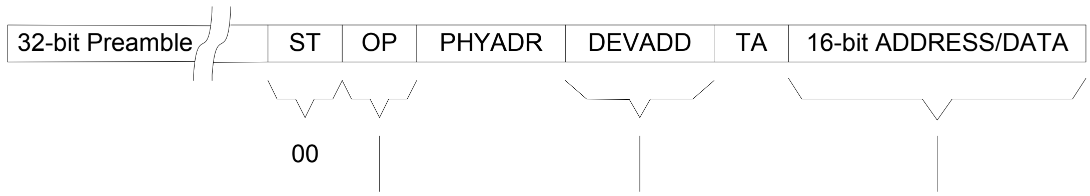


2.4 MDIO Management Frame Structure

CFP MDIO interface uses the communication data frame structure defined in IEEE 802.3 Clause 45. Each frame can be either an address frame or a data frame. The total bit length of each frame is 64, consisting of 32 bits preamble, and the frame command body.

The command body consists of 6 parts illustrated in *Figure 2 CFP MDIO Management Frame Structure*.

Figure 2 CFP MDIO Management Frame Structure



OP	ACCESS TYPE
00	Address
01	Write
11	Read
10	Post Read Inc Add

DEVADD	DEVICE TYPE
00000	Reserved
00001	PMA/PMD
00010	WIS
00011	PCS
00100	PHY XS
00101	DTE XS

Access Type	Content
Address	Reg Address
Write	Write Data
Read	Read Data
Read Inc	Read Data

ST = start bits (2 bits),
OP = operation code (2 bits),
PHYADR = physical port address (5 bits),
DEVADD = MDIO device address (or called device type, 5 bits),
TA = turn around bits (2 bits),
16-bit ADDRESS/DATA is the payload.

3 CFP REGISTER OVERVIEW

3.1 CFP Register Space

The total CFP register space (from 8000h to FFFFh) is logically divided into 8 pages with each page starting at even hex thousand, that is, 8000h, 9000h, A000h, …, F000h. Each page has 4096 addresses and is further divided into 32 tables. Each table has 128 CFP register addresses. Note that there is no physical boundary in between pages and tables. The sole purpose of this logical segmentation is for the convenience of CFP register space allocation and access control. The overview of the CFP register allocation is listed in *Table 2 CFP Register Allocation*.

3.2 Non-volatile Registers (NVRs)

CFP MSA specifies the starting address of all non-volatile registers at 8000h and it specifies 8 NVR tables for storing module ID information, setup data, and additional data stored by vendor and user. All NVR tables are implemented with lower 8-bit of space filled with data and the upper 8-bit of space reserved. A fully populated table shall require a maximum of 128 bytes of NVM to back up.

3.2.1 CFP NVR Tables

CFP MSA specifies CFP NVR 1 table for storing Basic ID data, CFP NVR 2 table for storing Extended ID data, CFP NVR 3 table for storing Network Lane Specific data. CFP NVR 4 table is allocated for storing Host Lane Specific data. Currently only the checksum of CFP NVR 3 is stored in CFP NVR 4 table.

3.2.2 Vendor NVR Tables

Vendor NVR 1 and Vendor NVR 2 tables are allocated for storing additional data that can be used by the vendor.

3.2.3 User NVR Tables

The User NVR 1 and User NVR 2 tables are allocated for module user to store data. User has the full read/write access to these tables.

3.2.4 NVR Content Management

All populated CFP NVR tables shall be backed up by physical non-volatile memory (NVM). On module Initialize, CFP NVR tables shall be uploaded with stored NVM values. CFP module vendor shall manage the content of CFP NVR tables.

The content and management of Vendor NVR tables and User NVR tables are subject to additional agreement between user and vendor.

3.2.5 User Private Use Registers

Starting at 8F00h, two additional tables are allocated for “User private use”. CFP MSA does not specify nor restricts the use of these tables. The use of these User Private Use Registers is subject to additional agreement between CFP module users and vendors.

Table 2 CFP Register Allocation

CFP Register Allocation					
Starting Address in Hex	**Ending Address in Hex**	**Access Type**	**Allocated Size**	**Data Bit Width**	**Table Name and Description**
0000	7FFF	N/A	32768	N/A	Reserved for IEEE 802.3 use.
8000	807F	RO	128	8	CFP NVR 1. Basic ID registers.
8080	80FF	RO	128	8	CFP NVR 2. Extended ID registers.
8100	817F	RO	128	8	CFP NVR 3. Network lane specific registers.
8180	81FF	RO	128	8	CFP NVR 4.
8200	83FF	RO	4x128	N/A	MSA Reserved.
8400	847F	RO	128	8	Vendor NVR 1. Vendor data registers.
8480	84FF	RO	128	8	Vendor NVR 2. Vendor data registers.
8500	87FF	RO	6x128	N/A	Reserved by CFP MSA.
8800	887F	R/W	128	8	User NVR 1. User data registers.
8880	88FF	R/W	128	8	User NVR 2. User data registers.
8900	8EFF	RO	12x128	N/A	Reserved by CFP MSA.
8F00	8FFF	N/A	2x128	N/A	Reserved for User private use.
9000	9FFF	RO	4096	N/A	Reserved for vendor private use.
A000	A07F	R/W	128	16	CFP Module VR 1. CFP Module level control and DDM registers.
A080	A0FF	R/W	128	16	MLG VR 1. MLG Management Interface registers.
A100	A1FF	RO	2x128	N/A	Reserved by CFP MSA.
A200	A27F	R/W	128	16	Network Lane VR 1. Network lane specific registers.
A280	A2FF	R/W	128	16	Network Lane VR 2. Network lane specific registers.
A300	A37F	R/W	128	16	Network Lane VR 3. Network Lane n Vendor Specific FAWS Registers.
A380	A3FF	RO	128	N/A	Reserved by CFP MSA.
A400	A47F	R/W	128	16	Host Lane VR 1. Host lane specific registers.
A480	ABFF	RO	15x128	N/A	Reserved by CFP MSA.
AC00	AFFF	RW	8x128	16	Common Data Block Registers
B000	BFFF	RW	4096	16	Allocated for OIF MSA-100GLH modules, See Section 6.
C000	FFFF	RO	4x4096	N/A	Reserved by CFP MSA

3.3 Volatile Registers (VRs)

Page A000h is allocated for volatile registers. CFP MSA specifies 4 VR tables for module configuration, control, and various DDM related functions. All VR registers are 16-bit data with unused bits reserved. A fully populated table requires a maximum of 256 bytes of physical memory. There is no NVM backup for VR registers but CFP MSA specifies their initial values.

3.3.1 CFP Module VR 1 Table

This table, starting at address A000h, contains command/setup, module control, lane control, Module state, FAWS (fault/alarm/warning/status), FAWS Summary, and other DDM related registers. All registers are assigned with initial values to insure the correct startup condition.

3.3.2 Network Lane Specific Register Table

Two tables starting from A200h and ending at A2FFh are allocated to support network lane specific registers including lane FAWS, controls, and A/D values (For copper network lanes some of the DDM register support may not apply.). For each supported register, CFP MSA allocates a 16-lane array for it. Should in the future more than 16 lanes are needed additional tables can be allocated in the subsequent reserved addresses.

3.3.3 Host Lane Specific Register Table

One table starting at A400h is allocated to support host lane specific registers. For each supported parameter, CFP MSA allocates a 16-lane array for it. Should in the future more than 16 lanes are considered additional tables can be allocated in the subsequent reserved addresses.

3.4 Module Vendor Private Registers

Page 9000h is reserved exclusively for module vendors of CFP module for their development and implementation needs.

3.5 Reserved CFP Registers

All reserved CFP registers and all the reserved bits in a CFP register shall be “read-only” and they shall be read as all-zeros. Writing to reserved CFP registers or bits shall have no effect. CFP registers related to unused lanes for a specific module type shall be treated as reserved CFP registers. An example would be CFP registers relating to network lanes 15:4 for a 100GBASE-LR4 module (in which only network lanes 3:0 are active).

3.5.1 Un-implemented Registers

A particular CFP module may not implement every function by this Specification. The registers or bits in the registers representing the un-implemented functions shall be read as 0. Writing to these registers or register bits has no effect.

3.6 CFP Register Data Types

A CFP register collects management information in a basic form of a 16-bit word, occupying one MDIO register address. CFP Registers support the following data types.

3.6.1 Byte

A byte can represent a signed number, unsigned number, or an array of 8-bit value. If a CFP register only contains one byte of data, it allocates the least significant 8 bits for it, with all most significant 8 bits reserved. All the non-volatile registers contain a byte with bit 7 being the most significant bit.

3.6.2 Word

A word is a 16-bit-wide data type. It can represent a signed number, unsigned number, or an array of 16-bit values. It can also be used as 2 bytes, the most significant byte and the least significant byte. The most significant byte occupies the bits from 15 to 8. The least significant byte occupies the bits from 7 to 0. All the volatile registers contain a word with bit 15 being the most significant bit.

3.6.3 Bit Field

A CFP register can contain one or more bit fields. A bit field consists of one or more bits, which can represent a number or an array of bit values. If a bit field represents a number the bit with the highest bit number is the most significant bit.

3.6.4 Two's Complement

Wherever signed byte is used, two's complement is assumed. *Table 3* illustrates the example bit patterns and values of a signed byte in two's complement form. For a 16-bit signed word, the same format applies with the most significant bit (bit 15) to be the sign bit. The value of +32767 = 7FFFh and the value of -32768 = 8000h.

Table 3 Bit Pattern of a Two's Complement Byte Data

BIT 7 (SIGN BIT)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0		VALUE
0	1	1	1	1	1	1	1	=	+127
0	0	0	0	0	0	0	1	=	+1
0	0	0	0	0	0	0	0	=	0
1	1	1	1	1	1	1	1	=	-1
1	0	0	0	0	0	0	1	=	-127
1	0	0	0	0	0	0	0	=	-128

4 CFP CONTROL AND SIGNALING THEORY

4.1 CFP Module States and Related Signals

To facilitate a well-defined CFP module startup and module turn-off sequences and other applications, CFP MSA specifies a list of CFP module states that CFP module shall support.

In association with these states, a set of signals that are related to state transitions are also defined. In the following text, a signal name with a lower-case "s" suffix stands for a combination of multiple signals.

4.1.1 Signals Affecting Transition of CFP Module States

Three inputs and one internally generated signal are defined and each of them is a logical combination of hardware signal status, CFP register bit status, and module internally generated logic signals in some cases. These signals affect the state transition.

4.1.1.1 Combined Module Reset Signal MOD_RSTs

For reset operation, CFP module internally defines MOD_RSTs as follows:
MOD_RSTs = (**NOT** MOD_RSTn) **OR** (Soft Module Reset) **OR** Vcc_Reset,
where,

MOD_RSTn is the hardware pin input,
Soft Module Reset is a CFP register bit, de-asserted in Reset and,
Vcc_Reset is the CFP internally generated logic signal indicating the validity of Vcc

Vcc_Reset = 1 if Vcc at connector is lower than a specified threshold,
= 0 if Vcc is within range.

Note that Vcc_Reset does not correspond to the operating voltage range specified in the CFP MSA Hardware specification. Vcc_Reset is the threshold voltage below which the module is held in reset, and above which normal operation can be initiated.

The threshold for Vcc_Reset is vendor specific and shall be lower than Vcc Low Alarm Threshold (808Eh).

4.1.1.2 Combined Module Low Power Signal MOD_LOPWRs

MOD_LOPWRs = MOD_LOPWR **OR** (Soft Module Low Power) **OR** HW_Interlock,
where,

MOD_LOPWR is the hardware pin input,
Soft Module Low Power is the CFP register bit, de-asserted in Reset, HW_Interlock is defined below.

4.1.1.2.1 HW_Interlock

HW_Interlock (hardware interlock) is an internally generated logic value, based upon the comparison between the module’s power class (Refer to Reference 5, Section 2.2.1.4 for power class definition) versus the host cooling capacity as encoded on the HW_IL_MSB and HW_IL_LSB input pins. Its purpose is to prevent an otherwise-dangerous high power condition which might harm either the host or the module itself, due to power requirements which the host is not able to support.

The status of HW_Interlock is defined as follows:
HW_Interlock = 0 if HW_IL_MSB and HW_IL_LSB = 11b or,
HW_Interlock = 0 if module power <= Host cooling capacity, else
HW_Interlock = 1 if module power > Host cooling capacity.

In operation, the module samples the status of the HW_IL_MSB and HW_IL_LSB input pins once during the Initialize State. To ensure a reliable sampling, Host shall hold HW_IL_MSB and HW_IL_LSB signal valid until the module exits Initialize State. The module stores these values in a variable HW_IL_inputs. (The Host is free to reprogram the usage of the PRG_CNTLn input pins and change their values at any time after the module exits the Initialize State.)

When both the MOD_LOPWR input pin and the Soft Module Low Power register bit are de-asserted, the module then compares the variable HW_IL_inputs to the power class for which it is designed (Defined in the Power Class field of register 8001h). The result of this comparison updates the HW_Interlock status. The module remains in the Low-Power State if HW_Interlock evaluates to '1' (this does not result in a transition to the Fault State). Conversely, if HW_Interlock evaluates to '0', the module is allowed to transition to the High-Power-up State.

Host capable to manage CFP2 module with power class > 3 are recommended upon MOD_ABS pin de-assertion to keep MOD_LOPWR input pin asserted.
When MOD_LOPWR state is reached, Host shall interrogate the module via MDIO bus and check whether CFP2 exact power class derived from 807Eh register is matching the Host cooling capacity. Only after a positive response from previous check the MOD_LOPWR input pin can be de-asserted from the Host.

4.1.1.3 Combined Transmitter Disable Signal TX_DISs

TX_DISs = TX_DIS **OR** (Soft TX Disable),

where,

TX_DIS is the hardware pin,
Soft TX Disable is a CFP register bit, de-asserted in Reset.

4.1.1.4 Fault Conditions

Fault conditions are represented by all the non-reserved bits except bit 0 in the Module Fault Status register. Each bit is driven by a particular fault condition through hardware or software means in CFP module. Any assertion of these bits causes the CFP module to enter the Fault state.

4.1.1.5 Minimum Signal Duration

The host shall provide the minimum assert/de-assert pulse width of 100 micro-seconds to guarantee the module to enter a transient state. The module's behavior for pulse width less than 100 micro-seconds is un-defined. (This clause is subject to removal per Group discussion. The timing of these signals shall be defined by CFP MSA HW Spec. – Editor)

4.1.2 Signals Affected by Module Insertion or State Transition

CFP MSA specifies a number of output signals, both in the form of hardware pins and CFP register bits, reporting to the Host the transitions between states. In most of cases, the hardware pins are mirrored with CFP register bits.

4.1.2.1 MOD_ABS

This is a hardware signal which reports the presence of an inserted CFP module to the Host. There is no MDIO register counterpart of it. For more information please refer to Reference 5.

4.1.2.2 GLB_ALRM

GLB_ALRM is a CFP internal signal that is the invert signal of GLB_ALRMn. The latter is the hardware signal, as an interrupt request to the Host, reporting FAWS occurrence during module operation. When the CFP module detects that any bit is asserted in CFP FAWS latch registers (A022h through A026h), it shall assert GLB_ALRM, provided that those latch bits are enabled by CFP FAWS enable registers (A028h through A02Ch). GLB_ALRM is cleared upon the Host reading corresponding latched CFP registers.

4.1.2.3 INIT_DONE

INIT_DONE is a CFP internally generated and used signal indicating the completion of module initialization. This signal is dedicated to module startup process and it is asserted upon exiting the Initialize state. This signal remains asserted until MOD_RSTs is asserted.

4.1.2.4 HIPWR_ON

HIPWR_ON is a CFP internally generated status signal represented by a CFP register bit. It is the logical OR of TX-Off state, Turn-TX-on state, Ready state, and TX-Turn-off. It is asserted when the module exits High-Power-up state and remains asserted whenever the module is not in the Low Power condition.

4.1.2.5 MOD_READY (Ready State)

MOD_READY is an alias of Ready State bit in Module State register. The Ready State bit is asserted when the module enters Ready state and remains asserted as long as the CFP module is in the Ready state.

4.1.2.6 MOD_FAULT (Fault State)

MOD_FAULT is an alias of Fault State bit in Module State register. The Fault State is asserted when the module enters Fault state and remains asserted as long as the CFP module is in the Fault state.

4.1.3 CFP Module States

CFP MSA specifies 10 CFP module states in the context of defining the startup, normal operation, and module turn-off sequences. Five of the 10 states are steady states and the rest are transient states. The behavior of input and output to a state, and the state itself shall be defined for the clear hand-shaking between the Host and the CFP module.

Host can read CFP Registers Module State and Module State Latch to determine the module state at the time of read, except in Reset State and Initialize State.

4.1.3.1 Reset State (Steady)

MOD_RSTs assertion causes CFP module to reset, including reset of any digital circuitry that may consist of module control function and any high speed circuitry if they are re-settable. In particular the MDIO interface will be held in a high impedance state. Therefore, the Host will read "FFFFh" from any CFP register addresses while a host write will have no effect.

In this state, all circuits are in low power mode and stay in reset whenever MOD_RSTs is asserted. The MOD_RSTs supersedes the status of other input such as MOD_LOPWRs and TX_DISs.

Module reset shall happen when MOD_RSTs is asserted, when 3.3 V power supply is turned on, or when CFP module is hot-plugged in to the connector. When CFP module is already in connector, MOD_RSTs assertion can be used to resolve any hardware hang-up, particularly a communication hang-up or other types of control hang-ups.

Reset state is a steady state and shall exit to Initialize State upon the de-assertion of MOD_RSTs.

4.1.3.2 Initialize State (Transient)

Upon entering this state, CFP module shall keep MDIO interface held at high impedance state during the initialization. All the host-reads return “FFFFh” and all the host-writes have no effect.

Upon the completion of initialization, all the NVRs are loaded with NVM values and VRs are initialized. Analog A/D Value Registers shall be read with live values. All the allowed FAWS registers shall contain valid data. CFP module shall then release the hold of MDIO interface and assert GLB_ALRM bit to alert the Host of this MDIO ready condition.

On the exit of initialization, the CFP module shall enter Low-Power State. If initialization fails, it shall enter Fault State. Initialize State is a transient state. The CFP MSA specifies the maximum initialization time to be 2.5 seconds.

4.1.3.3 Low-Power State (Steady)

CFP module enters and stays in the Low-Power state when MOD_LOPWRs is asserted. In Low-Power state, the MDIO interface and control circuits shall remain powered and fully functional. All other high-power consuming circuits shall be in low-power condition.

In this state, the PHYs are powered down and loop-back is not possible. The nAUI outputs shall go to a steady state (no transitions).

Low-Power state is a steady state and it shall exit to High-Power-up state upon the de-assertion of MOD_LOPWRs.

4.1.3.4 High-Power-up State (Transient)

The Host drives CFP module into High-Power-up state from Low-Power state by the transition of de-asserting MOD_LOPWRs. In this state CFP module powers up all the functional circuitry and completes all required initialization such as inrush current control, TEC temperature stabilization, etc.

Upon exiting the High-Power-up state, the module shall assert HIPWR_ON signal and then shall enter TX-Off state. If the powering up process fails CFP module shall enter the Fault state and de-assert HIPWR_ON.

High-Power-up is a transient state. The time it takes to complete the process varies from module to module depending upon applications. The vendor shall specify the application-specific value in Maximum High-Power-up Time CFP register.

In this state, the nAUI outputs are not defined.

4.1.3.5 TX-Off State (Steady)

CFP module enters and stays in the TX-Off state when TX_DISs is asserted. In TX-Off state, the transmitters in all the network lanes are turned off but all other parts of the module remain high powered and functional.

TX-Off state is a steady state and it shall exit to TX-Turn-on state upon the de-assertion of TX_DISs, or it shall exit to High-Power-Down state upon the assertion of MOD_LOPWRs or MOD_RSTs.

4.1.3.6 TX-Turn-on State (Transient)

The Host drives CFP module into TX-Turn-on state by the transition of de-asserting TX_DISs signal from TX-Off state.

Asserting TX_DISs causes a global action that turns off all the transmitters across all network lanes.

In this state, CFP module either enables or disables lanes according to the configuration in Individual Network Lane TX_DIS Control CFP register. The lanes that are disabled shall remain disabled after the module enters the TX-Turn-on state.

Changing TX_DISs does not affect Individual Network Lane TX_DIS Control CFP register. Upon successfully turning on the desired transmitters CFP module shall assert MOD_READY to inform the Host. The CFP module shall enter Ready state. If the turning on TX process fails due to any fault conditions CFP module shall enter the Fault state and keep MOD_READY de-asserted.

TX-Turn-on is a transient state. The time it takes to complete the TX-Turn-on process varies depending upon the applications. The vendor shall specify the Maximum TX-Turn-on Time CFP register.

4.1.3.7 Ready State (Steady)

CFP module enters from TX-Turn-on state and stays in Ready state upon successful transmitter turning on. In this state CFP module is ready for passing data. All the MDIO, DDM, and other functions are fully functional.

Ready state is a steady state and it shall exit to other states upon the assertion of MOD_RSTs, MOD_LOPWRs, TX_DISs, or Fault conditions.

4.1.3.8 TX-Turn-off State (Transient)

The Host drives CFP module into TX-Turn-off state by asserting TX_DISs, MOD_LOPWRs, or MOD_RSTs. In this state CFP module turns off all the network lane transmitters regardless the setting in Individual Network Lane TX_DIS Control register.

TX-Turn-off is a transient state. The time it takes to complete the turn-off shall meet the spec listed in *Table 8 Timing for Management Interface Control and Status*.

4.1.3.9 High-Power-Down State (Transient)

CFP module enters High-Power-down state by the transition of asserting MOD_LOPWRs or MOD_RSTs. In this state, CFP module powers down all the power-consuming circuitry to maintain the overall power consumption less than 2 Watts. CFP module shall maintain MDIO interface fully functional.

Upon powering down the module CFP module shall de-assert HIPWR_ON to inform the Host. The CFP module shall either enter Low-Power state or Reset state depending upon the status of MOD_RSTs.

High-Power-down is a transient state. The time it takes to complete this transient state shall meet the spec listed in *Table 8 Timing for Management Interface Control and Status*.

4.1.3.10 Fault State (Steady)

CFP module enters this state from any states except Reset state upon the assertion of bits in Module Fault Status register. On entry to this state, CFP module shall immediately de-assert MOD_READY.

In this state, the CFP management interface and DDM shall remain fully functional. The module shall be put in low power mode to avoid the possibility of permanent module damage. Further diagnosis of the failure can be conducted by interrogating CFP FAWS summary registers and other registers.

In this state, the PHYs are powered down and loop-back is not possible. The nAUI outputs shall go to a steady state (no transitions).

Fault state is a steady state, and it shall exit to Reset state upon the assertion of MOD_RSTs.

4.2 State Transition Diagram

The CFP module state transition is shown in *Figure 3 State Transition Diagram during Startup and Turn-off*. The top row of states and the associated transitions are typical of the CFP module startup sequence. The Host can control the power-on sequence by controlling the conditions of MOD_RSTn, MOD_LOPWR, and TX_DIS.

When TX_DISs is asserted in Ready state, CFP module shall enter the TX-Turn-off state and then transient to TX-Off state.

When MOD_LOPWRs is asserted in Ready state, CFP module shall enter TX-Turn-off state and High-Power-down states sequentially. And then it shall enter Low-Power state.

When MOD_RSTs is asserted in Ready state, CFP module shall first enter TX-Turn-off State and then High-Power-down State before entering Reset State.

When one or more fault conditions occur, CFP module shall enter the Fault State.

Behavior of the signals affected by module state transition is defined in *Table 4 Behavior of Signals Affected by Module State Transition*. Of the four signals listed in the table, GLB_ALRM drives the GLB_ALRMn pin. During module startup GLB_ALRMn signals the Host the completion of Initialization.

The signals HIPWR_ON, MOD_READY, and MOD_FAULT are CFP internally generated signals and are defaults of the programmable alarm pins PRG_ALRMx.

CFP register bits are allocated and can perform the same functions as the hardware control input pins. Additionally, Module State and Module State Latch registers provide the current module state and the state history.

Figure 3 State Transition Diagram during Startup and Turn-off

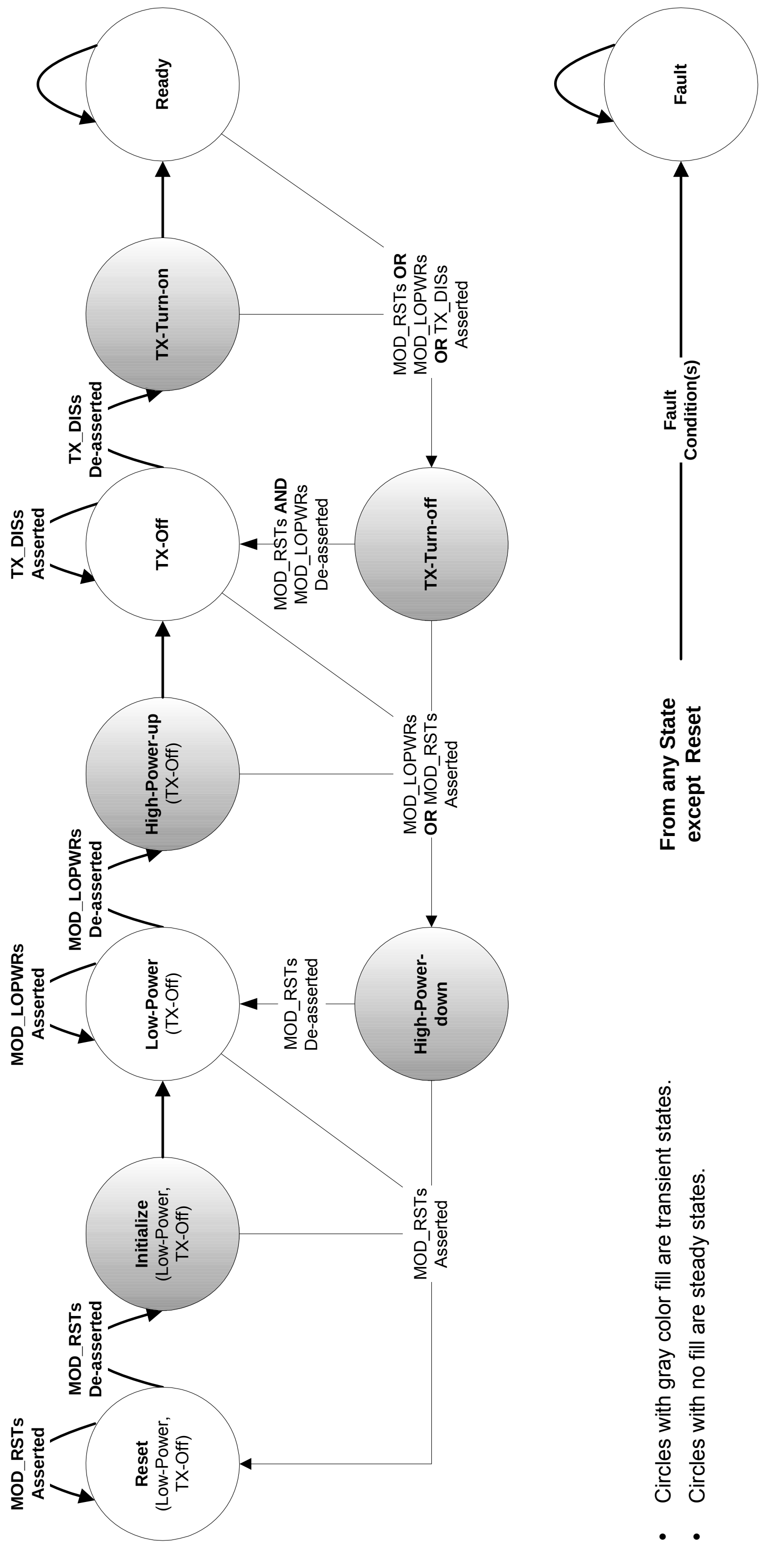


Table 4 Behavior of Signals Affected by Module State Transition

Signals	CFP Module State									
	Reset	Initialize	Low-Power	High-Power-up	TX-Off	TX-Turn-on	Ready	TX-Turn-off	High-Power-down	Fault
GLB_ALRM	D*	D*	A	A/D	A/D	A/D	A/D	A/D	A/D	A/D
HIPWR_ON	D*	D*	D	D	A	A	A	A	D	D
MOD_READY	D*	D*	D	D	D	D	A	D	D	D
MOD_FAULT	D*	D*	D	D	D	D	D	D	D	A
D* = De-asserted, guaranteed by internal hardware INIT_DONE signal. Note GLB_ALRM is the internal complement of GLB_ALRMn pin and it shall be de-asserted if MOD_RSTs is asserted. The HIPWR_ON, MOD_READY, and MOD_FAULT are defaulted to PRG_ALRM1, PRG_ALRM2, and PRG_ALRM3 pins respectively on module startup.										
A/D = Asserted or De-asserted depending upon Host's clear-on-read and Host-enabled status.										
A = Asserted.										
D = De-asserted.										

4.3 Examples of Module Startup and Turn-off Sequence

The examples below illustrate that the Host can control the module startup sequence by setting the initial conditions of MOD_RSTs, MOD_LOPWRs, and TX_DISs.

4.3.1 Power-up CFP Module to Ready State without Host Transition Control

Figure 4 Module Startup Sequence Example 1: No Host Transition Control illustrates CFP MSA specified module startup sequence for the Host to power up the CFP module to Ready state without the Host intervention. In this instance, the Host sets up the CFP module connector initial condition by applying Vcc to the connector and de-asserting MOD_RSTn, MOD_LOPWR, and TX_DIS.

The staggering arrangement of the connector pins (Reference 5) causes ground and Vcc to first contact CFP module. At the time when Vcc becomes available the pull-up/pull-down resistors in the module assert MOD_RSTn, MOD_LOPWR, and TX_DIS. As the "Plug-in" action progresses, MOD_RSTn and TX_DIS are in contact with the Host and hence they are de-asserted. Finally MOD_ABS and MOD_LOPWR are engaged. This causes MOD_LOPWR de-assertion. Hence the initial conditions the Host applies to the CFP module take effect.

The CFP module, under these initial conditions, goes through Reset, Initialize, High-Power-up, TX-Off, TX-Turn-on states, and finally enters Ready state. During this course, the CFP module asserts GLB_ALRM, HIPWR_ON, and MOD_READY signals sequentially. These signals inform host the completion of module initialization and MDIO availability, module fully powering up, and module ready, respectively.

MSA specifies two registers which contain Maximum High-Power-up Time and Maximum TX-Turn-on Time. Host uses these two parameters to determine how long it shall wait at each stage if reading HIPWR_ON and MOD_READY as the signals of progress monitor is not desirable or not available. Vendor shall provide these two register values as they may vary from product to product and from vendor to vendor.

4.3.2 Power-up the Module with Full Host Transition Control

In contrast to the case presented in 4.3.1, the Host can apply full control over the course of module power-up sequence. This example is illustrated by *Figure 5 Module Startup Sequence Example 2: Full Host Transition Control*.

4.3.3 Power-Up the Module with Some Host Transition Control

In some case, it is desirable to power up the module to Low-Power state. For this example, the Host may change PRG_ALRMs and PRG_CNTLs, before de-asserting MOD_LOPWR in the Low-Power State. This example is illustrated in *Figure 6 Module Startup Sequence Example 3: Some Host Transition Control*.

4.3.4 Example of Module Turn-off Sequence

Figure 7 Module Turn-off Sequence Example: No Host Transition Control illustrates the example of module turn-off sequence without the Host transition control by hot-un-plug. In this case, un-plug action causes assertions of MOD_ABS and MOD_LOPWR first. Then due to module extraction, MOD_RSTn is asserted. CFP module enters TX-Turn-off state and High-Power-down state subsequently. Between these events, CFP module de-asserts MOD_READY, HIPWR_ON, and GLB_ALRM sequentially and enters Reset. Finally Vcc is disconnected.

4.4 Special Modes of Operation

CFP MSA defines additional operation modes such as transmitting only and receiving only for a CFP module. CFP MSA specifies the standard operation mode is bi-directional. Uni-directional operation is optional (vendor-specific support). CFP register Module Enhanced Options register identifies what optional operation modes are supported for a particular module.

To power up the module in receiving only mode, the Host needs to assert TX_DIS and keeps other control signals as required. In this way CFP module will power up to TX-Off state and uses HIPWR_ON to inform the Host it is ready for receiving data. *Figure 8 Module Start-up Sequence Example: Operating in RX Only Mode* depicts this application. The support of transmitting only mode is no different from normal working mode except that the Host may expect CFP module to squelch the electrical outputs.

Figure 4 Module Startup Sequence Example 1: No Host Transition Control

NOTE: the following assumes the Host does not change the default register values

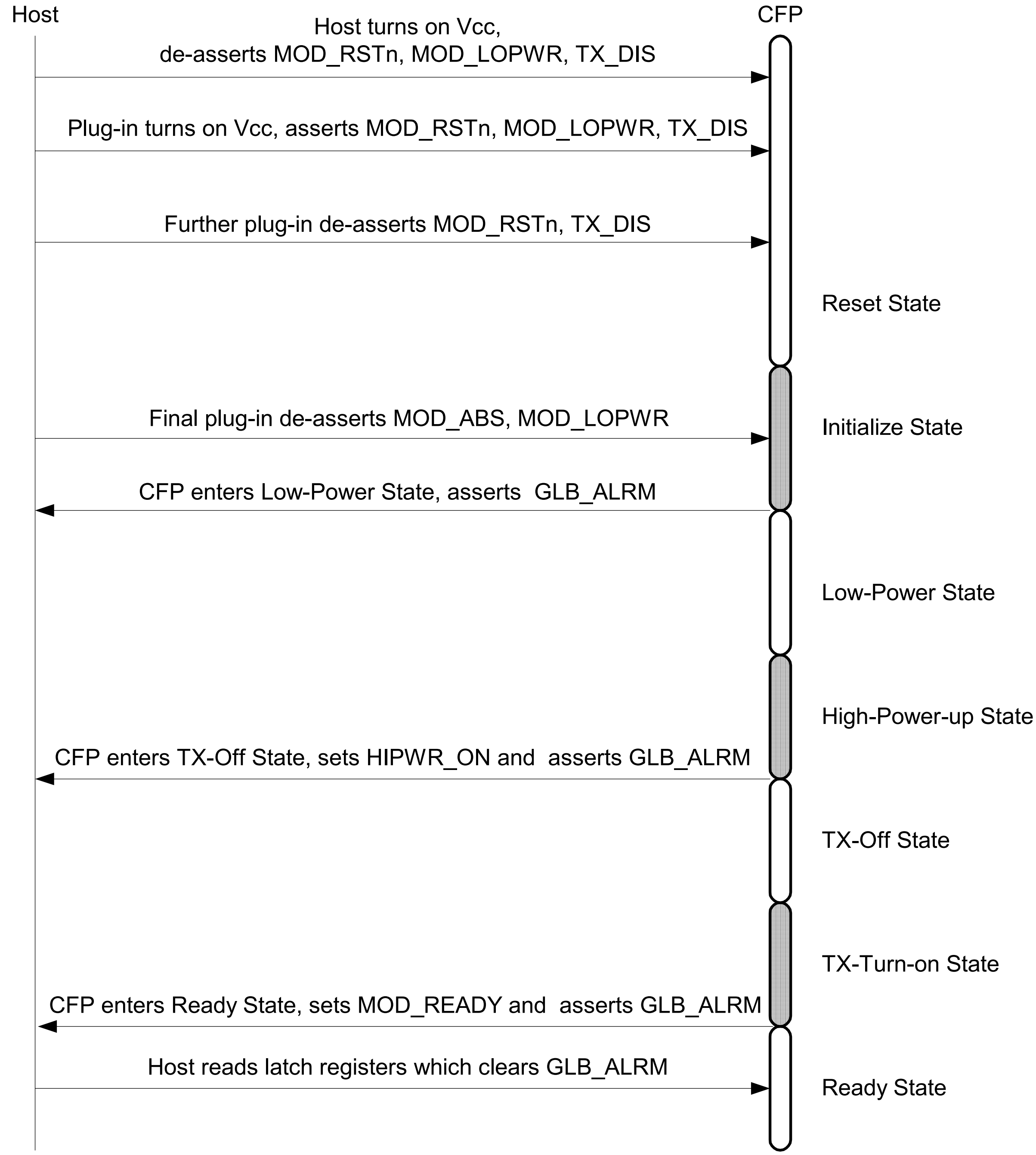


Figure 5 Module Startup Sequence Example 2: Full Host Transition Control

NOTE: the following assumes the Host does not change the default register values

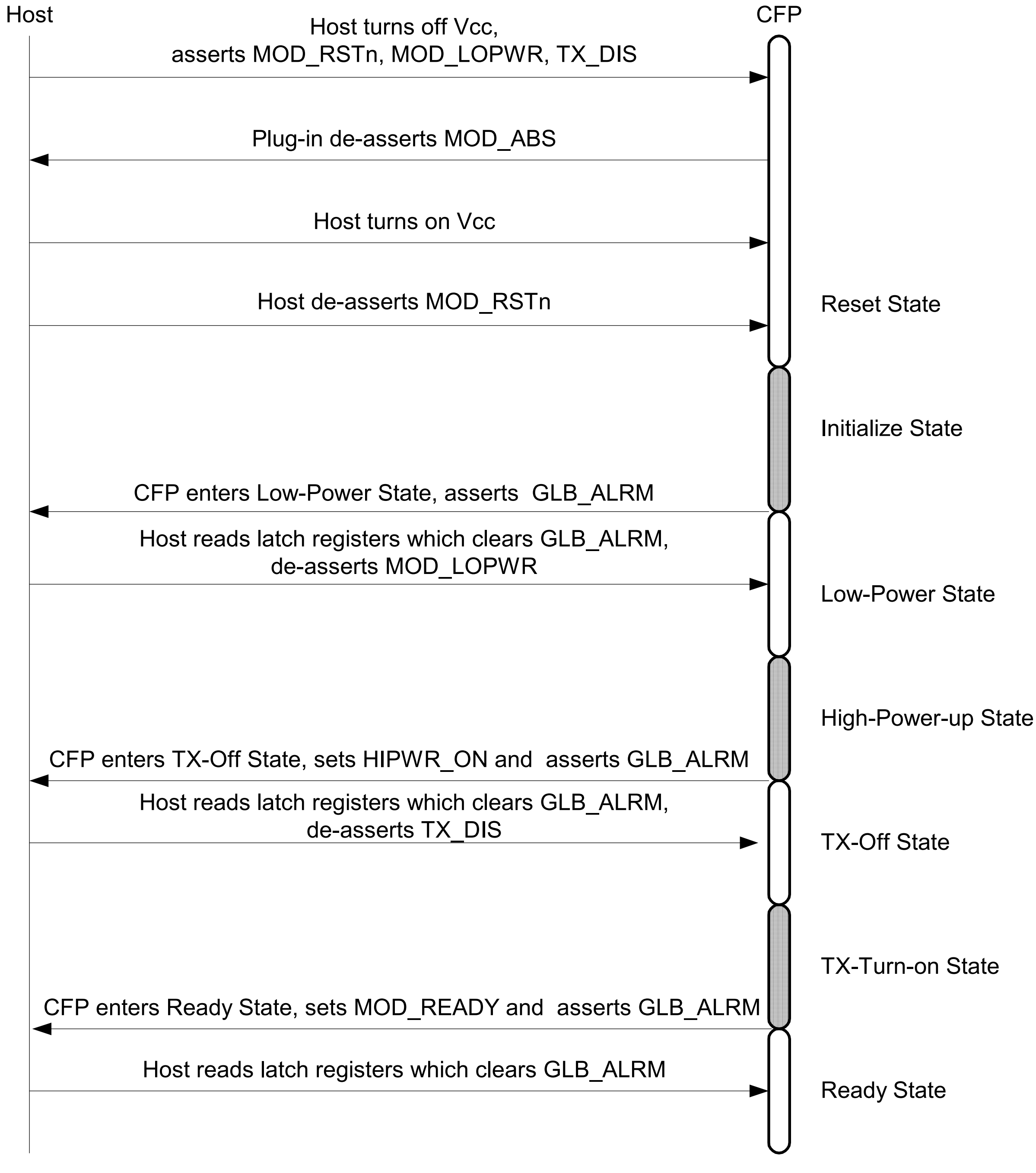


Figure 6 Module Startup Sequence Example 3: Some Host Transition Control

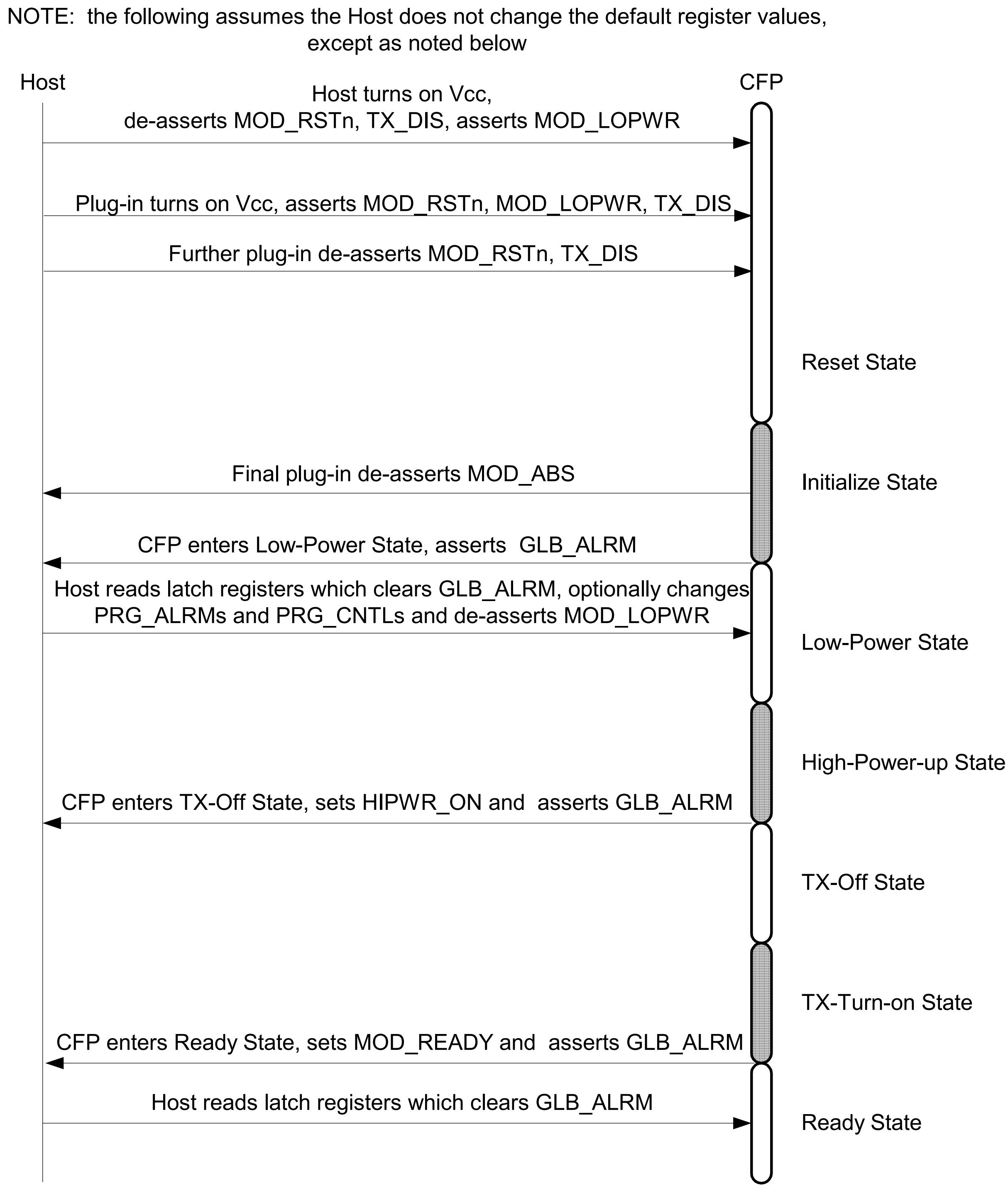


Figure 7 Module Turn-off Sequence Example: No Host Transition Control

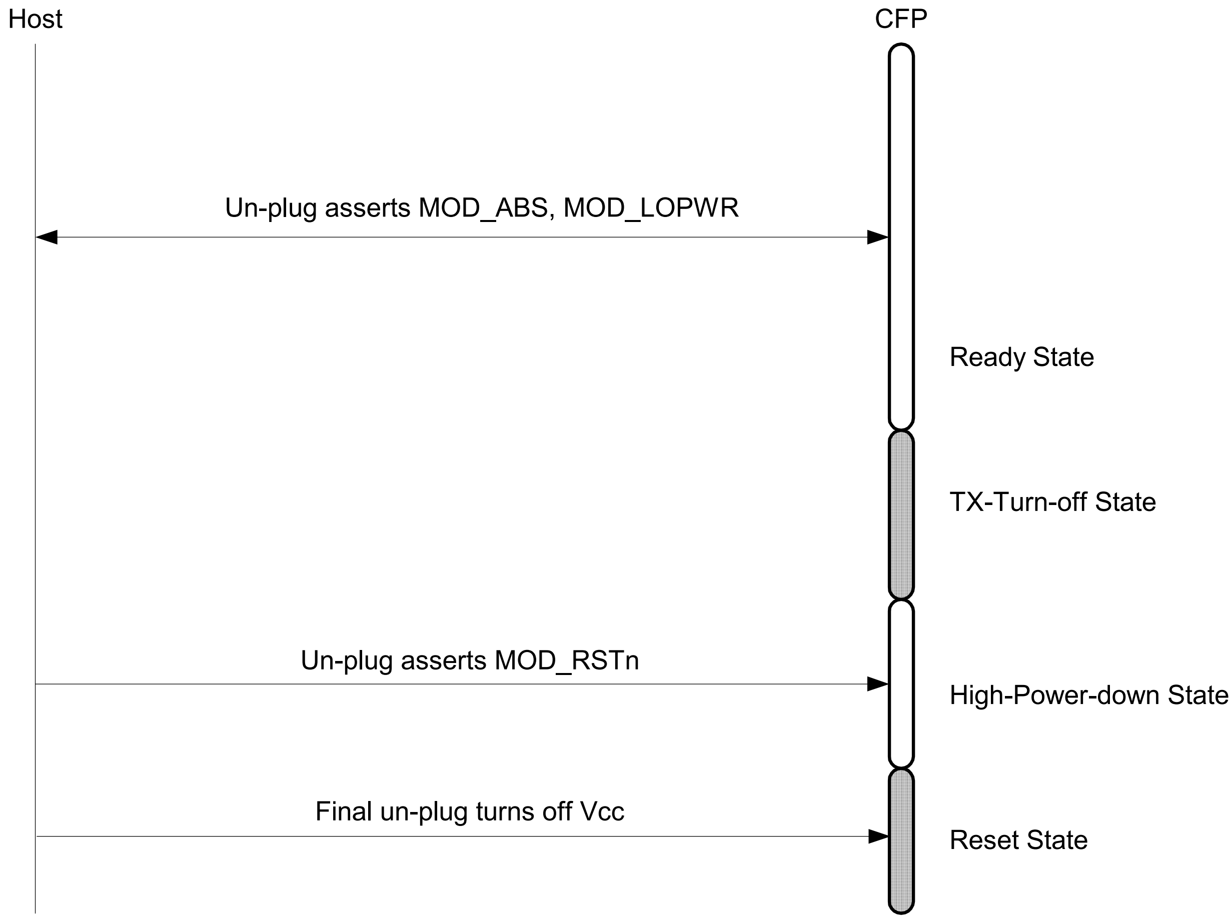
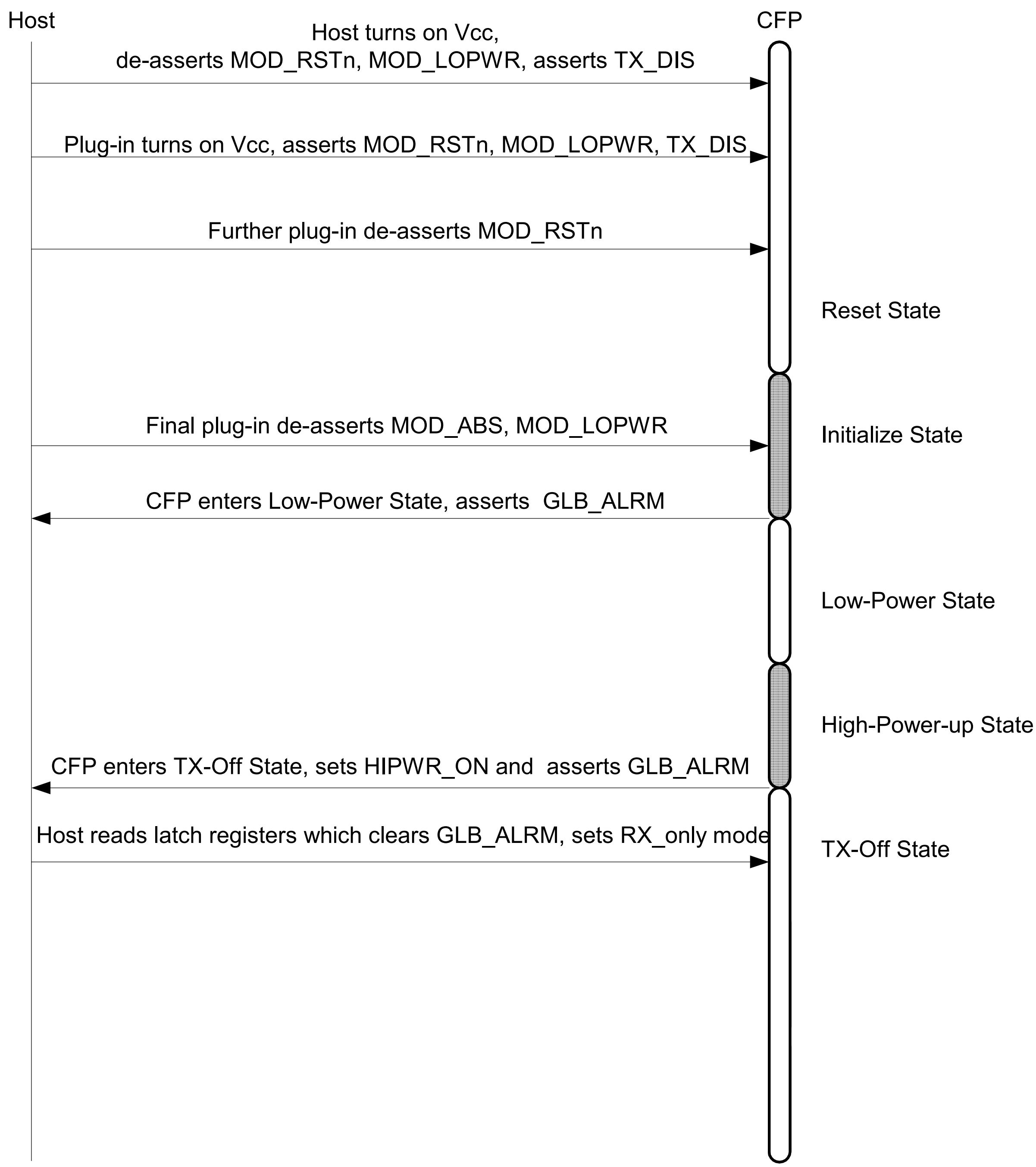


Figure 8 Module Start-up Sequence Example: Operating in RX Only Mode

NOTE: the following assumes the Host does not change the default register values



4.5 Behavior of FAWS in CFP States

CFP module shall eliminate the spurious FAWS signals in various CFP module states, based on a set of rules defined by CFP MSA. CFP MSA classifies all the GLB_ALRM contributing FAWS signals into three types: FAWS_TYPE_A, FAWS_TYPE_B and FAWS_TYPE_C. The type for each FAWS signal is annotated in *Table 27 CFP Module VR 1*, *Table 29 Network Lane VR 1*, and *Table 32 Host Lane VR 1*.

CFP MSA specifies the behavior of each FAWS type according to *Table 5 Behavior of FAWS Type in Different Module States*. Note that CFP module shall use FAWS_TYPE_[ABC]_ENA to eliminate any spurious FAWS reporting during state transition.

Table 5 Behavior of FAWS Type in Different Module States

FAWS Type	CFP Module State									
	Reset	Initialize	Low-Power	High-Power-up	TX-Off	TX-Turn-on	Ready	TX-Turn-off	High-Power-down	Fault
FAWS_TYPE_A	OFF	OFF	A	A	A	A	A	A*	A*	A
FAWS_TYPE_B	OFF	OFF	OFF	OFF	A	A	A	A*	OFF	A
FAWS_TYPE_C	OFF	OFF	OFF	OFF	OFF	OFF	A	OFF	OFF	A
A = FAWS sources are allowed (i. e. not masked). Status registers and latch registers are functional. A/D values reflect the actual measurements.										
A* = OFF if the MOD_RSTs is asserted.										
OFF = FAWS sources (status bits) are gated off by CFP module. As a result, the corresponding latch registers will not capture (latch) new events. Latch registers and Enable registers are kept un-changed from previous states. A/D values reflect the actual measurements, although they may not all be available in Low-Power State depending upon module implementation.										

Figure 9 FAWS Signal Model for a Single Bit illustrates the mechanism of a signal source contributing to the global alarm and the relationship between status, latch, and enable registers. In this figure, a set of CFP internal FAWS_[ABC]_ENA signals are used to control the behavior of each FAWS source signal. Note that Module State register is not subject to FAWS_[ABC]_ENA control.

4.6 Global Alarm System Logic

The CFP module uses GLB_ALRM, to alert the Host any condition outside normal operating conditions. The GLB_ALRM is related to all the contributing FAWS registers including the status registers, the latch registers, and the enable registers, all listed in *Table 6 Global Alarm Related Registers*.

Figure 9 FAWS Signal Model for a Single Bit

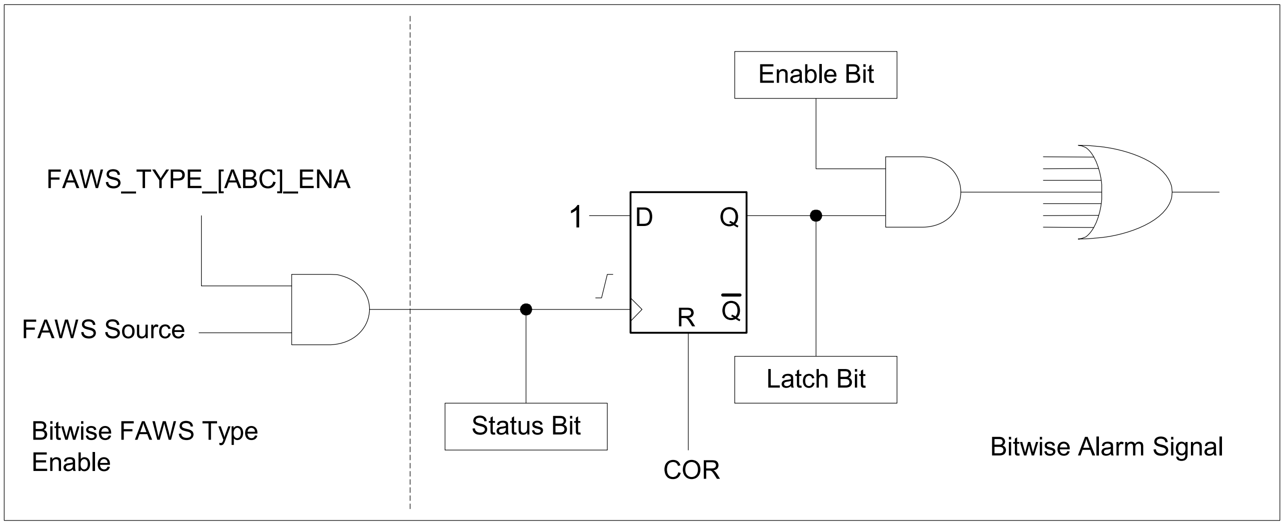


Figure 10 depicts the global alarm signal aggregation logic. In this system, status registers drive the latch registers on a bit-by-bit basis. The logic OR of all enabled bits in the latched registers drives GLB_ALRM. This simple and flat OR combinational logic minimizes the assert time after a global alarm condition happens.

Also shown in *Figure 10*, the Host shall control which latched bits resulting in a global alarm assertion by asserting individual bits in the enable registers. All enabling bits shall be volatile and startup with initial values defined in *Table 27 CFP Module VR 1*, *Table 29 Network Lane VR 1*, and *Table 32 Host Lane VR 1*.

When GLB_ALRM alerts the Host to a latched condition, the Host may query the latched registers for the condition. The latched bits are cleared on the read of the corresponding register. Thus a read of all latched registers can be used to clear all latched register bits and to de-assert GLB_ALRM.

In order to minimize the number of reads for locating the origin of the global alarm condition, the Host may use the global alarm query hierarchy listed in *Table 7 Global Alarm Query Hierarchy*.

Table 6 Global Alarm Related Registers

Description	**CFP Register Addresses**
Summary Registers	
Global Alarm Summary	A018h
Status Registers	
Module State	A016h
Module General Status	A01Dh
Module Fault Status	A01Eh
Module Alarms/Warnings 1	A01Fh

Module Alarms/Warnings 2	A020h
Network Lane Alarms and Warnings	A200h + n, n= 0, 1, …, N-1.
Network Lane Fault and Status	A210h + n, n = 0, 1, …, N-1.
Host Lane Fault and Status	A400h + m, m = 0, 1, …, M-1.
Latch Registers	
Module State Latch	A022h
Module General Status Latch	A023h
Module Fault Status Latch	A024h
Module Alarms/Warnings 1 Latch	A025h
Module Alarms/Warnings 2 Latch	A026h
Network Lane Alarms and Warnings Latch	A220h + n, n = 0, 1, …, N-1.
Network Lane Fault and Status Latch	A230h + n, n = 0, 1, …, N-1.
Host Lane Fault and Status Latch	A410h + m, m = 0, 1, …, M-1.
Enable Registers	
Module State Enable	A028h
Module General Status Enable	A029h
Module Fault Status Enable	A02Ah
Module Alarms/Warnings 1 Enable	A02Bh
Module Alarms/Warnings 2 Enable	A02Ch
Network Lane Alarms and Warnings Enable	A240h + n, n = 0, 1, …, N-1.
Network Lane Fault and Status Enable	A250h + n, n = 0, 1, …, N-1.
Host Lane Fault and Status Enable	A420h + m, m = 0, 1, …, M-1.
Notes: 1. “n” denotes the network lane index. 2. “N” is the total number of network lanes supported in a CFP module. The maximum value of N is 16. 3. “m” denotes the host lane index. 4. “M” is the total number of host lanes supported in a CFP module. The maximum value of M is 16.	

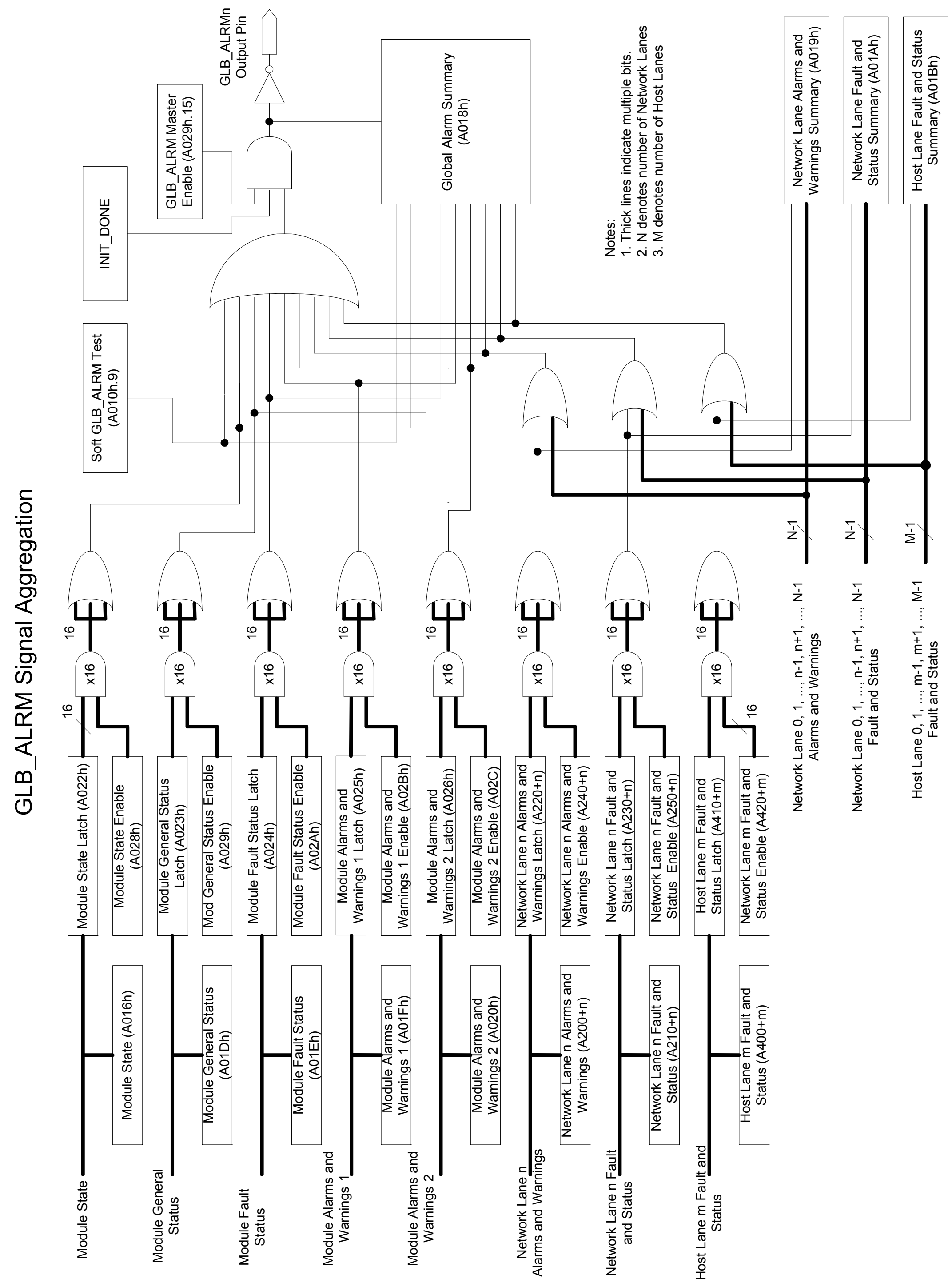
Table 7 Global Alarm Query Hierarchy

Query Level	CFP Register Name	CFP Register Addresses
1	Global Alarm Summary	A018h
2	Network Lane Alarms and Warnings Summary	A019h
2	Network Lane Fault and Status Summary	A01Ah
2	Host Lane Fault and Status Summary	A01Bh
3	Network Lane Alarms and Warnings Latch, lane n	A220h + n, n = 0, 1, …, N-1.
3	Network Lane Fault and Status Latch, lane n	A230h + n, n = 0, 1, …, N-1.
3	Host Lane Fault and Status Latch, lane m	A410h + m, m = 0, 1, …, M-1.
Notes: 1. “n” denotes the network lane index. 2. “N” is the total number of network lanes supported in a CFP module. The maximum N value is 16. 3. “m” denotes the host lane index. 4. “M” is the total number of host lanes supported in a CFP module. The maximum M value is 16.		

4.6.1 Latched and Summary Registers Synchronization

Latched registers and their parent summary registers shall be updated synchronously such that they are coherent in consecutive MDIO reads. For example, if an MIDO read detects a change in a summary register, a subsequent read to the reporting latched alarm register shall reflect the presence of the latched alarm condition.

Figure 10 Global Alarm Signal Aggregation



4.7 Specific Host Controls over Management Interface

4.7.1 Soft Module Reset (A010h.15) Function

Internal to CFP, this bit is logically OR'ed with both hardware pin MOD_RSTn and internally generated Vcc_Reset. This bit puts CFP module in Reset state when it is asserted by host. Once this bit is asserted by the Host it can only be cleared by CFP module. After a module reset caused by the assertion of this bit, CFP module exits Reset State if neither MOD_RSTn nor Vcc_Reset is asserted.

4.7.2 Soft Global Alarm Test (A010h.9) Function

This bit is provided for the host to forcibly assert the GLB_ALRM output, if desired. When GLB_ALRM function (refer to next paragraph) is enabled, asserting this control bit will assert the GLB_ALRM. This bit also directly feeds to Soft GLB_ALRM Test Status bit in Global Alarm Summary register for Host to verify the assertion of this bit.

The effect of this Soft Global Alarm Test bit can be verified by reading the GLB_ALRM State bit in Module General Status register. The GLB_ALRM Master Enable bit in Module General Status Enable register is provided as the master control to globally enable/disable GLB_ALRM. With this function Host does not need to change the settings of individual enable bits to disable the GLB_ALRM function.

4.8 Timing for Management Interface control and status reporting

Timing requirements for soft control, status functions and state transitions times are defined in *Table 8 Timing for Management Interface Control and Status*. For timing parameters related to the hard control and alarm pins refer to the CFP MSA Hardware Specification document.

Table 8 Timing for Management Interface Control and Status

Item	Parameter	Min	Max	Unit	Conditions
1	Soft Module Reset assert time		150	ms	Time from Soft Module Reset asserted[1] until CFP module enters Reset state.
2	Soft TX Disable assert time		150	ms	Time from the Soft TX Disable asserted[1] until all of the network lane optical (or electrical) outputs fall below 10% of nominal.
3	Soft TX Disable de-assert time		150	ms	Time from Soft TX Disable de-asserted[1] until the CFP module enters the TX-Turn-on State. The actual TX on time is this time plus the Maximum TX-Turn-on Time stored in CFP Register 8073h. The TX on time is when all of the network lane optical (or electrical) outputs rise above 90% of nominal.
4	Soft Module Low Power assert time		150	ms	Time from Soft Module Low Power asserted[1] until module enters High-Power-down state. The actual power down time is this time plus the Maximum High-Power-down Time stored in Register 8077h.

Item	Parameter	Min	Max	Unit	Conditions
					The power down time is when the total module power consumption less than 2 Watts.
5	Soft Module Low Power de-assert time		150	ms	Time from Soft Module Low Power de-asserted[1] until module enters High-Power-up State.
6	RX_LOS assert time		150	ms	Time from hardware RX_LOS pin asserted to RX_LOS Pin State (in A01Dh) asserted.
7	RX_LOS de-assert time		150	ms	Time from hardware RX_LOS pin de-asserted to RX_LOS Pin State de-asserted.
8	GLB_ALRMn assert time		150	ms	Time from any condition of FAWS alarm/status state to GLB_ALRMn asserted.
9	GLB_ALRMn de-assert time		150	ms	Time from last FAWS condition cleared to GLB_ALRMn de-asserted.
10	PRG_ALRM1 assert time		150	ms	Time from programmed FAWS condition occurrence to PRG_ALRM1 asserted.
11	PRG_ALRM2 assert time		150	ms	Time from programmed FAWS condition occurrence to PRG_ALRM2 asserted.
12	PRG_ALRM3 assert time		150	ms	Time from programmed FAWS condition occurrence to PRG_ALRM3 asserted.
13	PRG_ALRM1 de-assert time		150	ms	Time from programmed FAWS condition cleared to PRG_ALRM1 de-asserted.
14	PRG_ALRM2 de-assert time		150	ms	Time from programmed FAWS condition cleared to PRG_ALRM2 de-asserted.
15	PRG_ALRM3 de-assert time		150	ms	Time from programmed FAWS condition cleared to PRG_ALRM3 de-asserted.
16	PRG_CNTL1 assert time		150	ms	Time from PRG_CNTL1 asserted to programmed function to take effect.
17	PRG_CNTL2 assert time		150	ms	Time from PRG_CNTL2 asserted to programmed function to take effect.
18	PRG_CNTL3 assert time		150	ms	Time from PRG_CNTL3 asserted to programmed function to take effect.
19	PRG_CNTL1 de-assert time		150	ms	Time from PRG_CNTL1 de-asserted to the programmed function to cancel its effect.
20	PRG_CNTL2 de-assert time		150	ms	Time from PRG_CNTL2 de-asserted to the programmed function to cancel its effect.
21	PRG_CNTL3 de-assert time		150	ms	Time from PRG_CNTL3 de-asserted to the programmed function to cancel its effect.
22	MOD_FAULT assert time		150	ms	Time from the conclusion of any fault condition occurrence to MOD_FAULT asserted
23	HIPWR_ON assert time		150	ms	Time from module exiting High-Power-up state to HIPWR_ON asserted.
24	MOD_READY assert time		150	ms	Time from module entering Ready state to MOD_READY asserted.
1. Measured from the conclusion of Host write transaction.					

1

4.8.1 Miscellaneous Timing

Table 9 Miscellaneous Timing lists other timing parameters used in this Specification.

Table 9 Miscellaneous Timing

Item	Parameter	Min	Max	Conditions	Reference Clause
1	T_refresh	-	50 * (N+1) ms	DDM (A/D) data update rate. N = number of network lanes	2.3d, 5.5.8
2	T_assert	100 us	-	Minimum h/w input assertion time	4.1.1.5
3	T_initialize	-	2.5 s	From de-assertion of MOD_RSTs until the end of the Initialize State	4.1.3.2
4	T_high_power_up_max	-	Stored in NVR register 8072h	Max. time for the High-Power-up transient state to persist.	5.1.46
5	T_tx_turn_on_max	-	Stored in CFP NVR register 8073h	Max. time for the TX-Turn-on transient state to persist.	5.1.47
6	T_tx_turn_off_max	-	Stored in CFP NVR register 8076h	Max. time for the TX-Turn-off transient state to persist.	5.1.50
7	T_high_power_down_max	-	Stored in CFP NVR register 8077h	Max. time for the High-Power-down transient state to persist.	5.1.51
8	T_CDB_Timeout	-	150 ms	CDB Status stays	

4.9 Bit Error Rate Calculation

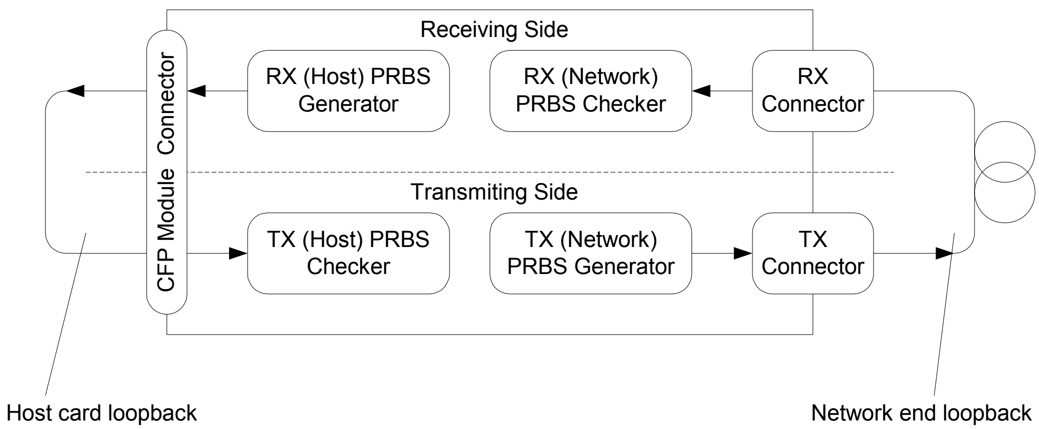
Optionally CFP module may have built-in PRBS generators and checkers. *Figure 11 CFP Built-in PRBS Components and Test Signal Flow* illustrates the relationship between these components and a loopback based test signal flow.

4.9.1 Network Lane PRBS Setup

CFP MSA specifies optional PRBS generator and error checker for each network lane with CFP register controls. To start a PRBS session, Host shall select the desired PRBS pattern by setting the Extended Tx Network Lane PRBS Modes Enable bit in the Module General Control 2 Register (A015.15) and the TX PRBS Pattern 1 and TX PRBS Pattern 0 bits in the Network Lane TX Control register (A011h.13~12). The Host enables the PRBS generators by asserting the bit TX PRBS Generator Enable in the same register (A011h.14).

Host shall apply the same operation to Network Lane RX Control register correspondingly to set up and enable the PRBS checker (A015.14 and A012.13~12). The PRBS generator and checker functions shall be stopped by de-asserting the TX PRBS Generator Enable and the RX PRBS Checker Enable (A012h.14), respectively.

Figure 11 CFP Built-in PRBS Components and Test Signal Flow



4.9.2 Network Lane BER Calculation

Upon assertion of RX PRBS Enable bit CFP module shall automatically set the Network Lane PRBS Data Bit Count and Network Lane PRBS RX Error Count (each per lane) to zero and shall start the accumulation. CFP module shall stop the accumulations for both data bit counting and error bit counting after RX PRBS Checker Enable is de-asserted. The counts shall be kept unchanged until RX PRBS Checker Enable is asserted next time.

The Host can read the Network Lane PRBS Data Bit Count and the per-lane Network Lane PRBS RX Error Count at any time. The bit error rate (BER) can be calculated by simply dividing the RX error count by data bit count. To achieve an accurate BER calculation, it is recommended that the Host reads these registers after PRBS Enable is de-asserted.

Both Network Lane PRBS Bit Count and Network Lane PRBS Error Count registers use an ad-hoc floating data format with 6-bit unsigned exponent and 10-bit unsigned mantissa. While the maximum count of this ad-hoc floating point number is 1023*2^63 ~= 2^73, CFP MSA specifies the effective maximum count to be 2^64 – 1 with a precision of 1/1024 in using this ad-hoc data format. Some examples in this data format are listed in *Table 10 CFP Ad-hoc Floating Point Number Examples*.

Table 10 CFP Ad-hoc Floating Point Number Examples

Count N (integer)	Mantissa (M)	Exponent (E)	Value Expression
0 ~ 1023	N	0	N * 2^0
1024 ~ 2047	N/2	1	(N/2) * 2^1
2048 ~ 4095	N/4	2	(N/4) * 2^2
4096 ~ 8191	N/8	3	(N/8) * 2^3

4.9.3 Host Lane PRBS Control

Host lane PRBS control is specified similar to that of network lane. The mechanism applies to RX PRBS Pattern 2, RX PRBS Pattern 1 and RX PRBS Pattern 0 in Host Lane Control register (A014h.6~44). The Host enables the PRBS generators by asserting the bit RX PRBS Generator Enable in the same register (A014h.7).

Host shall apply the same operation to Host Lane Control register (A014h.13~111 and A014h.14) correspondingly to set up and enable the PRBS checker. The host side PRBS generator and checker functions shall be stopped by de-asserting the RX PRBS Generator Enable and the TX PRBS Checker Enable respectively.

4.9.4 Host Lane BER Calculation

BER calculation for host lane is similar to that of network lane. In calculation, the Host shall use the Host Lane PRBS Data Bit Count register at A039h and the Host Lane PRBS TX Error Count registers at A430h through A43Fh.

4.10 CFP Register Access

4.10.1 Read and Write Accesses

Host shall have the read access to the registers or register bits that have Access Type of RO, RW, and COR on pages 8000h, A000h, and B000h.

Host shall have write access to the CFP registers or register bits that have Access Type of RW and WO on Pages 8000h and A000h Host writes to User NVRs results in volatile values which are stored in shadow registers.

Both Read and Write operations are conducted by directly using MDIO Command Frames.

4.10.1.1 4.10.1.1 Password Control (Optional)

Password control is optionally provided in CFP MSA MIS Version 2.2 to allow vendor and user control of access to information in the register shadow. Registers A000h ~ A001h are allocated for the password entry. If this option is not supported, these registers shall be read as 00000000h. Otherwise, these registers shall be read as FFFFFFFFh. Register access under password control is shown in *Table 11: Register Access Password Requirements*. If this option is not supported, any entries in the table that are not marked as N/A do not require a password.

When password control is supported, the password entry registers are write-only (WO) and shall always read FFFFFFFFh. Any values written to these registers are retained until Reset or rewritten by the host. Password is a 2-word long data with the most significant word occupying the lower register address. Password values for the user shall be in the range of 00000000h to 7FFFFFFFh. Password values for the vendor shall be in the range of 80000000h to FFFFFFFFh. MSA specifies the default user password value as 01011100h.

4.10.1.1.1 Power On/Reset Password Initialization

On power up and reset, the Password Entry registers shall be initialized to 00000000h. The initialized contents of the Password Entry registers are compared to the previously stored password value. If the previously stored password value is 00000000h, full access to password protected registers shall be allowed. Note that even though the internal contents of these registers have been initialized to 00000000h, a read of these registers by the host shall return FFFFFFFFh.

4.10.1.1.2 Password Entry

The password shall be entered by writing a value to registers A000h and A001h. If the contents of both registers match to the previously stored password value, full access to password protected registers shall be allowed. If the contents do not match to the previously stored password, any access to password protected registers shall not be allowed. In Version 2.2, CDB command Commit Password is specified. Host shall use this command to request confirmation of password entry validity from a module.

4.10.1.1.3 Password Change

The user password can be changed by writing the new value to the Password Change registers A002h and A003h after a password entry is successful. The new password value shall be stored and take effect only after writing the Save User Password command to register A004h. In MIS Version 2.2 CDB command Save New Password is specified. Host shall use this command to save user password to confirm the new password accepted by a module.

Table 11: Register Access Password Requirements

Register	Read	Write	Restore	Save	Note
Module NVR Tables	Not Required	N/A	N/A	N/A	1) Without an appropriate password, a read attempt shall get FFFFh. 2) Using register A004h tooperate
Vendor NVR Tables	Required[1]	N/A	N/A	N/A	
User NVR Tables	Required[1]	Required[1]	Required [1,2]	Required [1,2]	
Module VR Tables	Not Required	Not Required	N/A	N/A	

4.10.2 User NVR Restore and Save Functions

To write permanently to User NVR registers Host shall use the “Save” function to store the shadowed data into underlying NVM. The host only needs to perform a single Save operation to copy the entire User NVR shadow registers to the underlying NVM after finishing the editing the data. CFP MSA further specifies the minimum number of Save operation greater than 10,000 times.

Upon power-up or reset the User NVR shadow registers are “Restored” with NVM values. Restore function is also called to update the User NVR shadow registers with previously stored NVM values if the edited content of User NVRs is not desired. Note that the Restore function will overwrite the NVR shadow registers, losing any host-written values in them that have occurred since the last Save to the underlying NVM.

The NVR Access Control Register (A004h) provides the Restore and Save functions for Host to restore and save the User NVRs content. This register has a structure described in *Table 12 User NVRs Access Control Register (A004h)* and *Table 27 CFP Module VR 1*.

Table 12 User NVRs Access Control Register (A004h)

Access Type	Bit	Bit Field Name	Description[5]	Init Value
RW	15~9	Reserved	Vendor specific	0
RO	8~6	Reserved		0
RW[1]	5	Command[2]	0: Restore User NVRs 1: Save User NVRs	0
RO	4	Reserved		0
RO	3~2	Command Status[3]	00b: Idle, 01b: Command completed successfully, 10b: Command in progress, 11b: Command failed.	00b
RW[1]	1~0	Extended Command	00b ~ 01b: Vendor specific, 10b: Save User Password[4]. If bit 5 = 0, command has no effect. 11b: Restore/Save all User NVRs.	00b

1. Once a command has been invoked the values written to the “Command” and “Extended Command” bits are held until the RSC state machine transitions back to the idle state.
2. User writes to the User NVRs Access Control Register are not valid, except if an idle state is observed in Command Status. A read of this register after command completes is required to return to idle (reverts command status to 00b. Further commands should not be issued without returning to idle.
3. Command Status bits are mirrored to CDB Status (register AC00h.9~8). Command Status in A004h bits and CDB Status in AC00h must be synchronized.
4. Not recommended to use. It is recommended to use CDB command Save New Password to replace this implementation.
5. Register A004h is defined functionally similar to 0x8000 in Reference 3.

4.10.2.1 User NVR Restore and Save Command (Bit 5)

Bit 5 in NVR Access Control Register is designated for User NVR restore and save command (RSC). The execution of RSC is illustrated by *Figure 12 Restore and Save Command Execution State Diagram*. In an idle state any write transaction to the NVR Access Control Register shall initiate a User NVR transaction. A “0” written to bit 5 initiates a User NVR Restore. A “1” written to bit 5 initiates a User NVR Save. The extended command bits (1 and 0) determine the exact nature of the Save/Restore operation.

Only one command on User NVRs can execute at a time. If a command is initiated, the Command Status bits indicate “Command in Progress” in NVR Access Control Register and further writes to the NVR Access Control Register will be ignored.

A Soft Module Reset will be queued to avoid crashing the User NVRs and NVM. The Host should always read the NVR Access Control Register to ensure that Command Status is not set to Command In Progress before attempting to assert the MOD_RSTs.

4.10.2.2 Restore and Save Command State Definitions

Table 13 Restore and Save Command State Definitions defines the four states in the execution of RSC transitions. *Table 14 Restore and Save Command State Transitions* further defines the RSC state transitions when a Restore or Save command is executed.

Table 13 Restore and Save Command State Definitions

RSC STATE	When Entered
IDLE	Default state when no Save/Restore user NVRs are in progress.
CMD_PENDING	State where command is pending availability of system resources,
IN_PROGRESS	State assumed while User NVR restore or User NVR save is in process
CMD_COMPLETE	State assumed after User NVR restore or User NVR save has occurred but before outcome has been read from the Command Status bits.

Table 14 Restore and Save Command State Transitions

RSC State Transition	Invocation
From IDLE to CMD_PENDING	Initiated by a write to the NVR Access Control Register.
From CMD_PENDING to IN_PROGRESS	Occurs when system resources are free to execute the requested command.
From IN_PROGRESS to CMD_COMPLETE	Initiated by the NVR logic indicating that a User NVR restore or User NVR save operation has been completed.
From CMD_COMPLETE to IDLE	Initiated by a read of the NVR Access Control Register.

4.10.2.3 State Machine Function Definitions

The RSC state machine function definitions used in *Figure 12 Restore and Save Command Execution State Diagram* are as follows.

wr_A004h = MDIO write to NVR Access Control Register (A004h)
rd_A004h = MDIO read from NVR Access Control Register
exec(cmd_code) = perform command indicated by “cmd_code”

“cmd_code” defined by combination of bit 5 and bit 1:0 of NVR Access Control Register, or in the case of reset, it is “reset User NVR”.

4.10.2.4 Command Status (bits 3, 2)

Following a write to register A004h (initiation of Restore/Save command), bits 3 and 2 provide information on the status of the command. A value of 00b indicates an idle condition, 10b indicates that a command is pending or in progress, 01b indicates that the command completed successfully, and 11b indicates that the command failed.

4.10.2.5 Extended Commands (bits 1, 0)

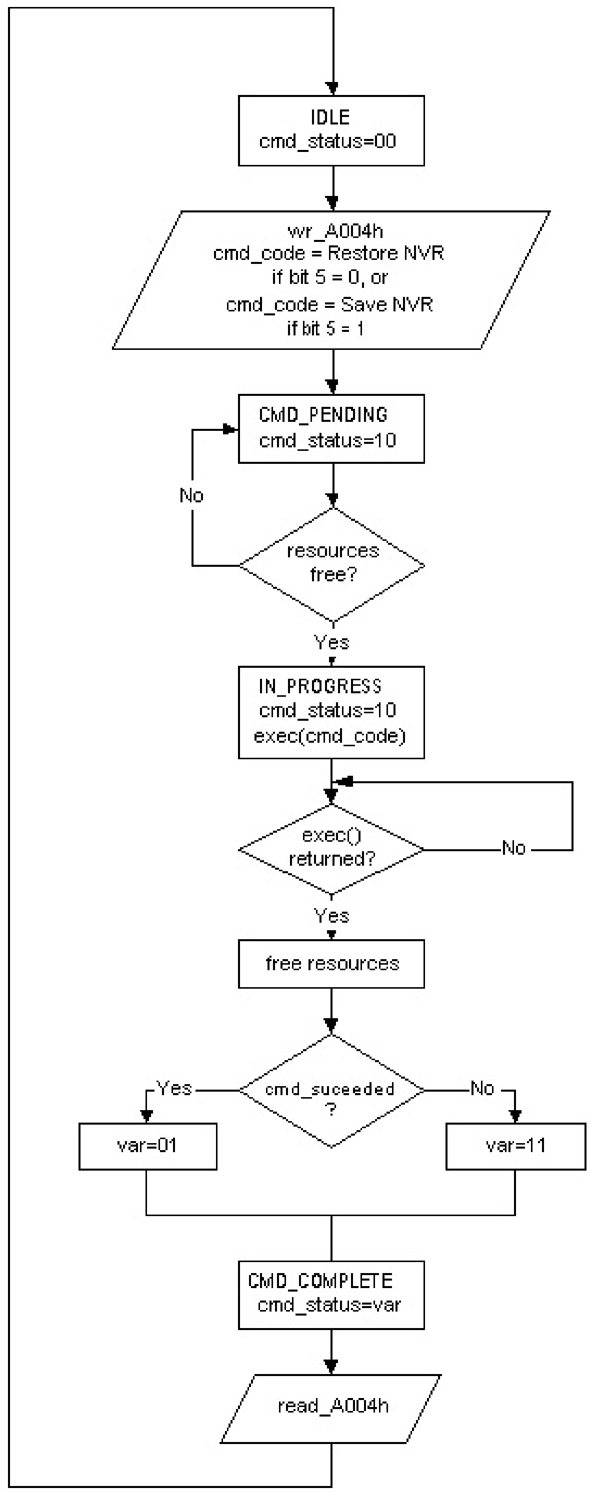
The register bits 1 and 0 supplement the basic RSC (bit 5) function. A value of 11b restores and saves all User NVR contents. A value of 10b saves User Password. All other values implement vendor specific commands.

4.10.2.6 NVR Data Safety in Save Function

The following conditions and measures shall be considered to avoid corrupting the user NVR when a Save Command is performed.

a) After a Save command is issued, the Host shall wait until the Command Status = Command Complete before performing any one of the operations of shutting down VCC, asserting MOD_RSTn, and asserting Soft Module Reset, otherwise the incomplete execution of Save command or NVR data corruption will be resulted.
b) The Host shall not expect a Save command to be accepted or executed when it is issued with a CFP module in Reset state or in Initialize state. When the module is in Fault state, it may or may not be able to complete the Save Command successfully, depending upon the nature of the fault.
c) Caution should be taken when hot-un-plug the CFP module as described in 4.3.4 “Example of Module Turn-off Sequence”. The sequence by the Host and by the CFP module cannot prevent the user NVR data corruption if a Save command is in progress and the module is hot-un-plugged by a user.

Figure 12 Restore and Save Command Execution State Diagram



4.11 Setup of Programmable Control and Alarm Pins

4.11.1 Relationship between HW PIN PRG_CNTLx, MDIO PRG_CNTLx Pin State, and MDIO PRG_CNTLx

Hardware pins PRG_CTRL2 and 3 are used for the hardware interlock function during Initialze State. After initialization, the pin functions follow PRG_CNTL2 and 3 Function Select setting (a005h, A006h). In this case the CFP operation and PRG_CNTL Pin State dependencies on hardware pin settings and Soft PRG_CNTL follow as defined in *Table 15 HW Pin PRG_CNTL1, PRG_CNTL1 Pin State, and SOFT PRG_CNTL*.

Table 15 HW Pin PRG_CNTL1, PRG_CNTL1 Pin State, and SOFT PRG_CNTL

	PRG_CNTL1 (Hardware pin)	PRG_CNTL1 Pin State (Register A010h.1)	Soft PRG_CNTL1 (Register A010h.10)	CFP Operation
A	1=high (Normal)	1	0 (Normal)	Normal
B	1=high (Normal)	1	1 (Reset)	Reset
C	0=low (Reset)	0	0 (Normal)	Reset
D	0=low (Reset)	0	1 (Reset)	Reset

4.11.2 Programmable Control Functions for PRG_CNTLs

Each programmable control pin can be programmed with the functions defined in *Table 16 Programmable Control Functions*.

Table 16 Programmable Control Functions

NAME	FUNCTION	VALUE
TRXIC_RSTn	Reset TX and RX ICs, PRG_CNTL1 MSA default.	0: Normal, 1: Assign TRXIC_RSTn function to any of the 3 hardware pins PRG_CNTL3, PRG_CNTL2, and PRG_CNTL1. When so assigned these hardware pins use the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, their soft counterparts Soft PRG_CNTL3, Soft PRG_CNTL2, and Soft PRG_CNTL1 (A010h.12~10) use an active high logic, that is, 1 = Assert (Reset).

4.11.3 Programmable Alarm Sources for PRG_ALRMs

Each programmable alarm pin can be programmed with the alarm sources defined in *Table 17 Programmable Alarm Sources*.

Table 17 Programmable Alarm Sources

NAME	ALARM SOURCE	VALUE
HIPWR_ON	Module high-power-on indicator. PRG_ALRM1 MSA default.	0: Module not high powered up, 1: Module high power up completed.
MOD_READY	MOD_READY, module startup sequence done, PRG_ALRM2 MSA default.	0: Not done, 1: Done.

MOD_FAULT	Fault detected. PRG_ALRM3 MSA default.	0: No Fault, 1: Fault.
RX_ALRM	Receive path alarm = RX_LOS + RX_LOL.	0: No receive path alarm, 1: Receive path alarm asserted.
TX_ALRM	Transmit path alarm = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL.	0: No transmit path alarm, 1: Transmit path alarm asserted.
RX_LOL	RX IC Lock Indicator.	0: Locked, 1: Loss of lock.
TX_LOSF	Transmitter Loss of Signal Functionality.	0: All transmitter signals functional, 1: Any transmitter signal not functional
TX_LOL	TX IC Lock Indicator.	0: Locked, 1: Loss of lock.
OOA	Host lane skew out of alignment indicator.	0: No OOA, 1: Out of alignment.

4.12 Common Data block

CFP MSA MIS Version 2.2 specifies a Common Data Block (CDB) in Page A000h by modifying the Bulk Data Block structure introduced in MIS 2.0 that supports OIF 100G DWDM LH modules. In Version 2.2 CDB is specified to use the same block of registers for multiple new applications. It presents to the host the same set of registers interface for different applications and meantime it reliefs the module from the burden of maintaining the growing number of registers.

With CDB, CFP MSA MIS 2.2 shall support the following new functions for CFP/CFP2 /CFP4 modules.

- Write flow control mechanism needed for new registers (refer to 6.2.3)
- Multiword read with data coherency (6.2.5.3)
- Bulk data transfer from host to module or from module to host (6.2.9)
- Module firmware upgrade capability (6.2.6)
- New applications that require extensive number of registers
- New applications that require complex procedures

4.12.1 CDB Structure

CFP MSA MIS 2.2 allocates 1024 registers on A000h page as the CDB starting at AC00h and ending at AFFFh. *Figure 13 Common Data Block Structure* illustrates that CDB has two realizations, the CDB Command Frame (Panel A) and the CDB Reply Frame (Panel B). When host requests module to perform a task it writes a CDB Command Frame to the module. When host requests the status of last command execution with optional data return it reads a CDB Reply Frame from the module.

4.12.1.1 CDB Command Frame

4.12.1.1.1 CDB Command Register

In a CDB Command Frame AC00h contains the CDB Command which is required to make a valid command frame. Host shall write to this register as the last register to write in a Command Frame. Writing to this register "triggers" the execution of the CDB Command by module.

4.12.1.1.2 CDB Payload Size Register

CDB Payload Size register is at AC01h containing the total number of registers of CDB Payload starting at AC02h. The minimum value of CDB Payload Size is 1 and the maximum value is 1020. Zero value indicates that the payload is not present. Payload Size register shall be always present regardless of its value.

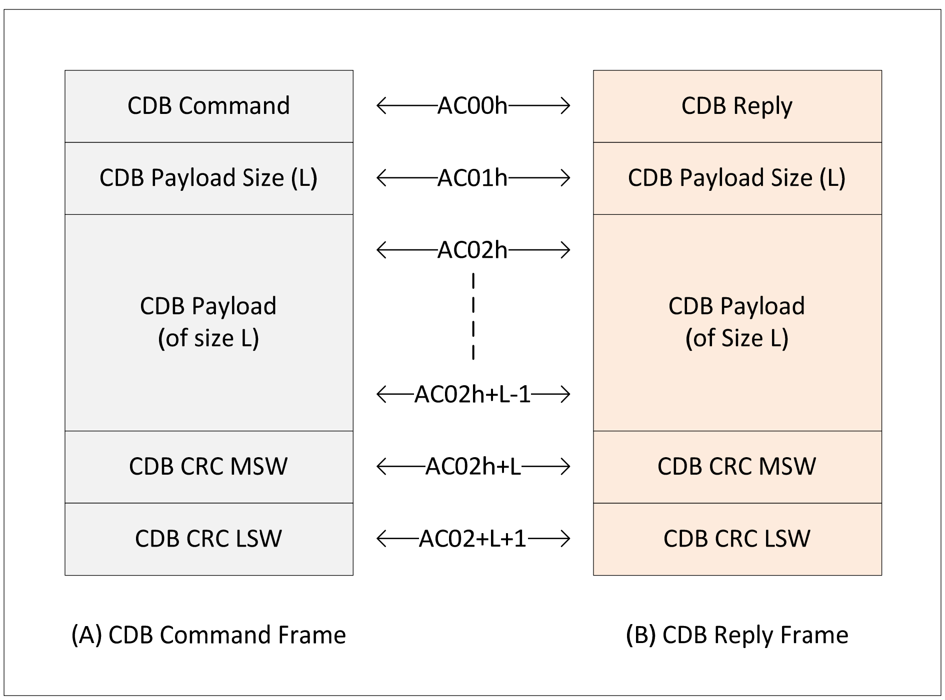
4.12.1.1.3 CDB Payload Registers

CDB Payload occupies a block of registers starting at AC02h and ending at AC02h+L-1, where L is the CDB Payload Size. CDB Payload contains parameters or other type of data associated with a CDB Command. CDB Payload is only present when CDB Command has data to pass to the module.

4.12.1.1.4 CDB CRC Registers

The CRC registers are allocated right after the end of CDB Payload with MSW at smaller address. CRC is a 32-bit value with the same algorithm defined for B000h page Bulk Data Block. The use of CRC is optional but it is used they always shall start at AC02h.

Figure 13 Common Data Block Structure



4.12.1.2 CDB Reply Frame

In a CDB Reply Frame AC00h contains the CDB Reply required to make a valid reply frame. Host shall read this register first to determine where it needs to read further for the rest of the Reply Frame. When preparing a Reply Frame a module shall write to this register with "Command in Process" in the field of CDB Status indicating the rest of the Reply Frame may not be ready for host to read. The rest of a CDB Reply Frame is similar to that of a CDB Command Frame.

4.12.2 CDB Implementation

Table 18 CDB Implementation specifies the general form of CDB Command Frame and CDB Reply Frame with implementation details.

Table 18 CDB Implementation

Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name***	***Description***	***Initial Value***
AC00	**1**			**CDB Command or CDB Reply**	**This is a shared address between CDB Command register and CDB Reply register, defined respectively with the following cases.**	**0000h**
		CDB Command Frame Case				
		WO	15~12	Reserved		0
		WO	11~8	CDB CMD Class	A 4-bit unsigned value coding 16 CDB Command Classes. 0h: System level operations 1h: General CFP register operations 2h~Dh: Reserved Eh~Fh: Vendor specific command class code.	0
		WO	7~0	CDB CMD Code	An 8-bit value coding 256 CDB commands for each CDB CMD Class. See separate section for details.	0
		CDB Reply Frame Case				
		RO	15~10	Reserved		0
		RO	9~8	CDB Status	A 2-bit value representing CDB status. Note this field shall be synchronized with A004h.3~2 therefore CDB and A004h can be operated one and only one at a time. 00b: CDB Idle, 01b: CDB Command completed successfully, 10b: CDB Command in progress, 11b: CDB Command failed.	0

			7~0	CDB Message	An 8-bit value coding CDB Message related to each CDB Status.
					If CDB Status = CDB Idle, then
					00h: Reserved,
					01h: Ready to accept host command,
					02h~7Fh: Reserved by MSA,
					80h~FFh: Allocated for vendor use.
					If CDB Status = Command in Progress, then
					00h: Reserved,
					01h: Command is captured but not processed,
					02h: Command checking is in progress, CDB Reply CRC is not valid.
					03h: Command execution is in progress,
					04h: Command execution is in progress but CDB Payload is open for host write, note that write to CDB Command register (AC00h) shall be ignored. Meanwhile, Payload Size and CRC in the Reply Frame may be overwritten by incoming host write.
					05h~7Fh: Reserved by MSA,
					80h~FFh: Allocated for vendor use.
						0

Hex Addr	*Size*	*Access Type*	*Bit*	*Register Name*	*Description*	*Initial Value*

					If CDB Status = CDB Command Completed Successfully, then
					00h: Reserved,
					01h: No specific message, one more host read gets CDB to idle status,
					02h~3F: Reserved by MSA,
					40h~7Fh: For individual CDB Command or task progress report ,
					80h~FFh: Allocated for vendor use.
					If CDB Status = Command Failed, then
					00h: Reserved,
					01h: CDB Data Length error, L > 1020,
					02h: Unknown command,
					03h: Command checking error without detail,
					04h: Command checking time out,
					05h: CRC error,
					06h: Password error,
					07h~0Fh: Reserved for CDB command checking error,
					10h: Command execution error without detail,
					11h~3Fh: Reserved by MSA
					40h~7Fh: For individual CDB command or task error,
					80h~FFh: Allocated for vendor use.	

AC01	**1**			**CDB Payload Size**	Contain the length of CDB Payload.	**0000h**
		RO	15~10	Reserved		0
		RW	9~0	Payload Size	A 10-bit unsigned integer L, 0= < L <= 1020.	0
AC02	**L**	**RW**	15~0	**CDB Payload**	**Data block of size L with either a CDB Command or Reply.**	**N/A**
AC02+L	**2**	**RW**	15~0	**CDB CRC**	**32-bit CRC for the registers AC00h, AC01h, and CDB Payload. Most significant word at smaller address.**	**0000h**

4.12.2.1 Write Flow Control on CDB

Write flow control (WFC) applies to CDB for secured communication between host and module. The field of CDB Status of CDB Reply Register AC00h.9~8 shall be used by host to realize the WFC. *Table 19 Write Flow Control to CDB Registers* presents the details of operation.

Table 19 Write Flow Control to CDB Registers

CDB Status =	**CDB Message Value =**	**Host Write to CDB**	**Host Read from CDB**
CDB Idle	Any value	Okay.	Allowed.
CDB Command Completed Successfully	Any value	No effect.	Allowed, one CDB Reply read shall bring to CDB Idle
CDB Command in Progress	01h, 02h, 03h	No effect.	Allowed.
CDB Command in Progress	04h	Allowed and effective except no effect on AC00h.	Allowed.
CDB Command Failed	Any value	No effect.	Allowed, one CDB Reply read shall bring to CDB Idle.

4.12.2.2 CDB Message

In addition to write flow control, a CDB Message field is specified as part of CDB Reply. Host shall use this field to obtain additional information from module regarding command checking or command execution.

4.12.2.3 Password Control
Some CDB commands require password control to write if password option is activated.

4.12.2.4 Interaction with Register A004h
The write accesses to CDB Command register and A004h are mutually exclusive by synchronizing A004h.3~2 with AC00h.9~8. Write to other CDB registers shall be always allowed regardless the state of A004h.3~2.

4.12.2.5 Interrupt to Host
In addition to host reading CDB Reply register, module shall trigger GLB_ALRMn upon CDB Status change from CDB Idle to either Command Completed Successfully or Command Failed. Global Alarm Summary A018h.4 is allocated to reflect the CDB Status change. Note that Command In Progress and CDB Idle shall not trigger GLB_ALRMn.

CDB Interrupt to host is optional. It can be turned on and off by CDB Commands. Refer to *Table 21 CDB Command Table* for details. Upon power up the CDB interrupt to host is turned off. CDB Interrupt to host shall be cleared when CDB returns to CDB Idle status due to host reading CDB Reply register.

4.12.2.6 CRC Option
CRC option can be turned on and off by CDB Commands. Refer *Table 21 CDB Command Table* for details. When CRC option is chosen it applies to all the registers including AC00h, AC01h, and the whole CDB Data Block.

4.12.2.7 Initialization
On power up CDB function shall be initialized to CDB IDLE state with CRC and Global Alarm disabled.

4.12.3 CDB Command Execution

4.12.3.1 Host to Write a CDB Command Frame
To send a CDB Command to module host shall write CDB Command register AC00h at last and shall use this write as the “trigger” for module to execute the CDB Command. Host shall be able to write all other registers in a CDB Command Frame in any order. A module shall interpret other register contents per the CDB command once it detects the “trigger”.

4.12.3.2 Host to Read a CDB Reply Frame
To receive a CDB Reply Frame host shall read CDB Reply register (AC00h) first and then shall proceed with reading CDB Payload Size register and CDB Payload, and then CRC. If no data is return per the previous command, host only needs to read the CDB Reply register to determine the CDB Status and CDB Message. If the CRC option is off, then there is no need to read the CRC registers.

4.12.3.2.1 Command in Progress (CIP)
CIP is an important status for module to present to host. Once a command is received CDB state machine shall immediately update CDB Reply register with this status and

associated CDB Message. During this state, module shall not be able to determine its CRC content if CRC option is enabled. Host shall not make attempt to read CRC registers.

4.12.3.2.2 Command Completed Successfully (CCS)

CCS is asserted by a module with proper CDB Message for additional information. If CDB Payload is attached as a part of the CDB Command execution host shall read the CDB Payload per CDB Payload Size register. If CRC is enabled host shall read CRC registers as well to determine whether a valid CDB Reply Frame is valid.

4.12.3.2.3 Command Failed (CF)

CF is a CDB State indicating a failed execution of a CDB Command. The CDB Message shall be used by a module to provide additional cause of failure.

4.12.3.3 CDB Command Execution Process

CDB Command execution is an interactive process between host, CDB State Machine, and module processor. *Figure 14 CDB Command Execution Flowchart* illustrates the process of host execution. Note that CDB Reply is used extensively in CDB Command execution process.

4.12.4 CDB Commands and Applications

Host shall deploy one or more CDB Commands to request a task performed by a module. When a task consists of multiple commands CDB Message shall be employed to report the progress of a task. A multi-command task shall be described by defining some specific CDB Commands and a flowchart or a section of pseudo-code that defines the procedure by which multiple CDB Commands are called.

CDB Commands are listed in *Table 21 CDB Command Table* where all the acronyms used are listed in *Table 20 Acronyms used in CDB Command Table*.

4.12.4.1 Single Command Task

A single command application shall be implemented with one Command Frame write and multiple Reply Frame reads. Examples of this type of CDB Command include Password Commit, Password Save, Bulk Data Read, etc. Their usage is self-explanatory in the Command Table.

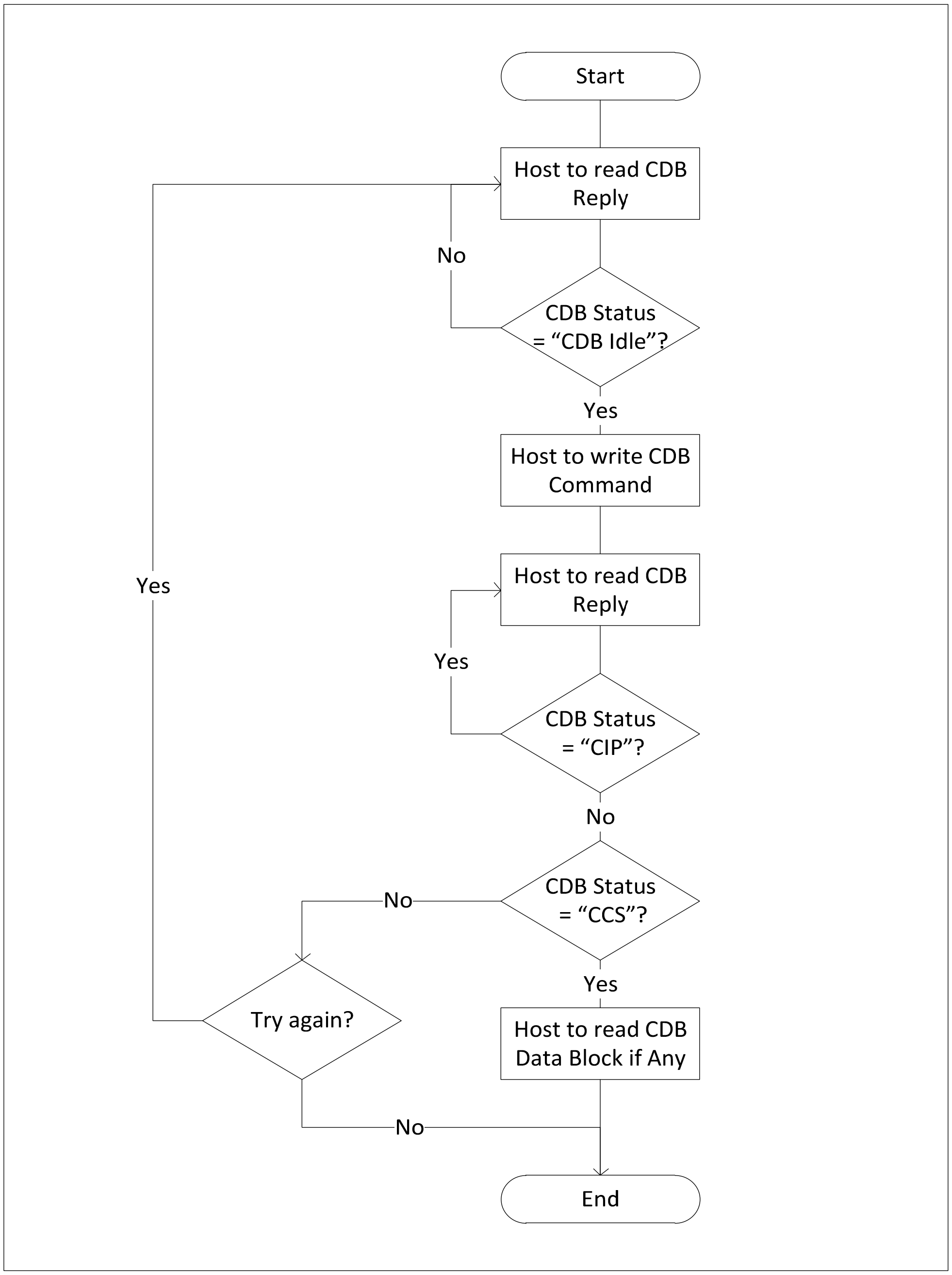
4.12.4.2 Multiple Command Task

A multiple command application shall be implemented with multiple Command Frame writes and multiple Reply Frame reads, executed in an order designed pertinent to a specific application. Examples of this type of applications include Firmware Field Upgrade, Module Authentication, etc.

4.12.4.2.1 Firmware Upgrade

Firmware upgrade procedure can refer *Figure 19 Software Upgrade State Machine* and *Figure 20 Software Upgrade Sequence* with exception that copy commands are not supported.

Figure 14 CDB Command Execution Flowchart



4.12.5 CDB Command Table

Table 20 Acronyms used in CDB Command Table

Acronym	Description
PW	Password
PS	Payload Size
PLx	Payload xth entry

Acronym	Description
Y	Yes or OK
N	No or None
CMD ID	Value in register AC00 in a CDB Command Frame. It is also used as a Command ID.

1 *Table 21 CDB Command Table*

CMD Class	CMD Code	CMD ID	Command Name	PS	PW	Description
CDB Command Class 0 – System Operation						
00h	00h	0000h	Reserved			
00h	01h	0001h	Commit Password	0	N	Commit to the password entered in A000h~A001h.
00h	02h	0002h	Save New Password	0	Y	Save the new password entered in A002h~A003h.
00h	03h	0003h	Enable Password	0	N	Enable the optional password protection for user NVR.
00h	04h	0004h	Disable Password	0	Y	Disable the optional password protection for user NVR.
00h	05h	0005h	Enable CDB CRC	0	N	Enable the optional CRC for CDB. This Command is volatile after power cycle. No CRC checking shall be executed on this command itself but CRC shall take effect starting from next CDB Command/Reply Frame if this command is executed successfully.
00h	06h	0006h	Disable CDB CRC	0	N	Disable the optional CRC for CDB. CRC checking shall be performed for this command itself but CRC shall be inactive starting from next CDB Command/Reply Frame.
00h	07h	0007h	Enable CDB Global Alarm Interrupt	0	N	Enable CDB Interrupt to host option. This Command is volatile.
00h	08h	0008h	Disable CDB Global Alarm Interrupt	0	N	Disable CDB Interrupt to host option.
00h	11h	0011h	Start Firmware Download	0	Y	Request the module to receive new firmware image with forth coming Bulk Data Write command. (Simulate B04Dh.15~12:1) Expected CMD specific Reply: 0140h: Ok to receive FW image, 0340h: Not enough NVM space, 0341h: Other errors.
00h	12h	0012h	Complete Firmware Download	0	Y	Request module FW image download is finished. (Simulate B04Dh.15~12: 2) Expected CMD specific Reply: 0140h: Full image has been received and image is good. 0340h: Image is incomplete, 0341h: Image is complete but CRC error,
00h	13h	0013h	Run Image A	0	Y	Request module to run Image A. (Simulate Bo4Dh.1~12: 3) Expected CMD Specific CDB Reply: 0140h: Command has been executed; 0340h: Image A is not valid, execution aborted. 0341h: other errors.
00h	14h	0014h	Run Image B	0	Y	Request module to run Image B. (Simulate B04Dh.15~12:4) Expected CMD Specific CDB Reply: 0140h: Command has been executed; 0340h: Image B is not valid, execution aborted. 0341h: other errors.
00h	15h	0015h	Abort Image Download	0	Y	Abort Image Download. (Simulate B04Dh.15~12:5). Expected CMD Specific CDB Replay: 0140h: Image download aborted.

CMD Class	CMD Code	CMD ID	Command Name	PS	PW	Description
						0340h: Command error.
00h	16h	0016h	Copy Image A to B	0	Y	Request module to copy Image A to B (Optional) Expected CMD specific CDB Reply: 0140h: Command has been executed; 0340h: Not enough memory, execution aborted. 0341h: Copying is not successful, 0342h: Other errors.
00h	17h	0017h	Copy Image B to A	0	Y	Request module to copy Image B to A (Optional) Expected CMD specific CDB Reply: 0140h: Command has been executed; 0340h: Not enough memory, execution aborted. 0341h: Copying is not successful, 0342h: Other errors.
00h	18h	0018h	Commit Image A	0	Y	Request module to commit to Image A. Expected CMD Specific CDB Reply: 0140h: Committed to Image A. 0340h: Command error.
00h	19h	0019h	Commit Image B	0	Y	Request module to commit to Image B. Expected CMD Specific CDB Reply: 0140h: Committed to Image B, 0340h: Command error.
00h	20h	0020h	Get Software Upgrade Status	0	Y	Get Firmware Upgrade Status. Host issues this command to get CDB Reply with a CDB Reply payload of size 1. Expected Reply: 0140h: Status read successful 0340h: Status read error Payload PL0 takes the identical definition as register B051h. Note the following fields of B051h are not included: B051h.15~14.
00h	21h	0021h	Download Image Block	L	Y	Host to download a block of software image to module. PL0 = Image Block Number (max 65535). The rest of CDB Payload is the software image block which can contain additional descriptor per vendor design. Note total image size is limited to 1019 x 65536 = 66.78 MB. Expected CMD specific Reply: 0140h: Image download successful. PL0 = Block number just downloaded. 0340h: CRC image block CRC error. PL0 = Block number just downloaded.
CDB Command Class 1 – Register Access						
1h	01h	0101h	Multiple Register Read	2	Y	Host to L registers with one command. PS = total size of payload. PL0=initial address, PL1= number of register to read counting from initial address.
1h	02h	0102h	Multiple Register Write	L+2	Y	Host to write L registers. PL0=Initial address, PL1=number of register to write, PL2 and on: register content.
1h	03h	0103h	Bulk Data Read	1	Y	Host to read L registers from module. PL0=Bulk data batch number or a descriptor specified by vendor.
1h	04h	0104h	Bulk Data Write	L+1	Y	Host to write L registers to module. PL0=Bulk data batch number or a descriptor specified by vendor.
1h	05h	0105h	Selected Register Read	L	Y	Host to read a set of L registers to be read at specified addresses. PL0 ~ PL(N-1) contains register addresses of the registers to be read.
1h	06h	0106h	Selected Register Write	2L	Y	Host to write a set of L registers to module at specified

CMD Class	CMD Code	CMD ID	Command Name	PS	PW	Description
						addresses. PL0~PL(2N-2) contain register address and content pair with address at odd PL number and content at even PL number sequentially.

4.13 Multi-link Gearbox (MLG) Support (optional)

Optionally CFP module may support MLG implementation. This paragraph is based on the document Multi-link Gearbox Implementation Agreement 1.0 which defines an in-band coding that allows independent 10GBASE-R signals to transit 10:4 gearboxes implementing a 100GBASE-R PMA function.

Registers A080h~A0FFh define the MLG1.0 generic management interface, MLG1.0 mux management interface and MLG1.0's demux management interface. For further information, please refer to document *IA OIF-MLG-01.0*.

5 CFP REGISTER DESCRIPTION

The detailed CFP register descriptions are listed in *Table 23 CFP NVR 1* through *Table 32 Host Lane VR 1*. Each table has 7 columns with the following definition.

Table 22 Table Column Description

Column	Description
Hex Addr.	MDIO address in hex number format For multi-register Data Field, it represents the lowest address of the field.
Size	Number of CFP registers in a given Data Field.
Access Type	RO = Read Only; RW = Read and Write; LH = Latched High[1]; COR = Clear On Read[2]; SC = Self Clearing.
Bit	This field indicates the range of bits used for a particular field in the format of m~n, where m is starting high bit and n is the ending low bit.
Register Name	This is the name of a register. Full English words are used for maximum clarity. Acronym use is minimized.
Bit Field Name	This is the name of a specific bit data field. Full English words are used for maximum clarity. Acronym use is minimized. Normally in non-bold face.
Description	Details of each Register field and/or behavior of a bit.
LSB Unit	This column contains the unit of a physical quantity represented by the least significant bit of the register field.
Init Value	The initial value that each volatile registers takes after the module boots up or is reset.

1. Latch registers are set on the rising edge of the associated status signals.
2. Clear-on-Read bits are cleared to 0 upon Host-read, independent of the condition of the (unlatched) status signal.

5.1 CFP NVR 1 Table: Base ID Registers

The 8000h page Base ID Registers defined in *Table 23 CFP NVR 1* are designed to support CFP modules. Note that in Version 2.2 of this document, CFP NVR 1 Table also supports MSA 100GLH modules.

In CFP MSA MIS Version 2.2 to save space and reduce errors, sections 5.1.1 through 5.1.56 have been merged with the descriptions of corresponding register in *Table 23 CFP NVR 1*.

Table 23 CFP NVR 1

CFP NVR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***LSB Unit***
				Base ID Information		
8000	**1**	**RO**	**7~0**	**Module Identifier**	**00h: Unknown or unspecified, 01h: GBIC, 02h: Module/connector soldered to motherboard, 03h: SFP, 04h: 300 pin XSBI, 05h: XENPAK, 06h: XFP, 07h: XFF, 08h: XFP-E,**	**N/A**

CFP NVR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***LSB Unit***
					09h: XPAK, 0Ah: X2, 0Bh: DWDM-SFP, 0Ch: QSFP, 0Dh: QSFP+, 0Eh: CFP, 0Fh: CXP (TBD), 10h: 168-pin 5”x7” MSA-100GLH, 11h: CFP2, 12h: CFP4, 13h ~ FFh : Reserved.	
8001	**1**	**RO**		**Extended Identifier**		**N/A**
			7~6	Power Class	This field defines Power Classes for CFP, CFP2, and CFP4, used together with hardware interlocking pins. Extended power classes are defined in 807Eh. Reference 5 CFP Hardware Spec for additional details. For CFP2 modules if power class > 3, see Section 4.1.1.2.1 for recommended power up sequence. The above definition is not applicable to MSA-100GLH modules. See 8182h for more.	N/A

Bits 7~6 Value	Power Class	CFP	CFP2	CFP4
00b	1	≤ 8 W	≤ 3 W	≤ 1.5 W
01b	2	≤ 16 W	≤ 6 W	≤ 3 W
10b	3	≤ 24 W	≤ 9 W	≤ 4.5 W
11b	>3	> 24 W	> 9 W	> 4.5 W

Hex Addr	Size	Access Type	Bit	Register Name / Bit Field Name	Description	LSB Unit
			5~4	Lane Ratio Type	00b: Network lane : Host lane = 1 : n (Mux type), 01b: Network lane : Host lane = n : m (Gear Box type), 10b: Network lane : Host lane = n : n (Parallel type), 11b: Reserved.	N/A
			3~1	WDM Type	A 3-bit field identifying any optical grid spacing used by CFP module000b: Non-WDM, 001b: CWDM, 010b: LANWDM, 011b: DWDM on 200G-grid, 100b: DWDM on 100G-grid, 101b: DWDM on 50G-grid, 110b: DWDM on 25G-grid, 111b: Other type WDM.	N/A
			0	CLEI Presence	0: No CLEI code present, 1: CLEI code present.	N/A
8002	**1**	**RO**	**7~0**	**Connector Type Code**	**00h: Undefined, 01h : SC, 07h : LC, 08h : MT-RJ, 09h : MPO, 0Dh : Angled LC, Other Codes : Reserved.**	**N/A**
8003	**1**	**RO**	**7~0**	**Ethernet Application Code**	**Any CFP module which supports an application which includes Ethernet and additional applications such as SONET/SDH, OTN, Fibre Channel or other, shall record the value in Ethernet Application Code as follows. 00h: Undefined type, 01h: 100GE SMF 10km, 100GE-LR4, 02h: 100GE SMF 40km, 100GE-ER4, 03h: 100GE MMF 100GBASE-SR10, 04h: 100GE MMF 100GBASE-SR4, 05h: 40GE SMF 10km, 40GE-LR4, 07h: 40GE MMF 40GBASE-SR4, 0Dh: 40GE-CR4 Copper 0Eh: 100GE-CR10 Copper, 0Fh: 40G BASE-FR,**	**N/A**

CFP NVR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***LSB Unit***
					10h: 100GE SMF 80km, 100GE-ZR1 **11h: 100GE DWDM, 100GE-DWDM-Coherent** **12h~FFh: Reserved.**	
8004	**1**	**RO**	**7~0**	**Fiber Channel Application Code**	**Any CFP module which supports an application which includes Fibre channel and additional applications such as SONET/SDH, OTN, Ethernet or other, shall record the value in Fibre channel Application Code as follows.** **00h: Undefined type.** **01h~FFh: Reserved.**	**N/A**
8005	**1**	**RO**	**7~0**	**Copper Link Application Code**	**In this CFP register, the CFP module shall identify what if any non-Ethernet Copper based PMD application which is supported. At the time of the writing, this application is undefined.** **00h: Undefined type.** **01h~FFh: Reserved.**	**N/A**
8006	**1**	**RO**	**7~0**	**SONET/SDH Application Code**	**Any CFP module which supports an application which includes SONET/SDH and additional applications such as Ethernet, OTN, Fibre channel or other, shall record the value in SONET/SDH Application Code as follows.** **00h: Undefined type,** **01h: VSR2000-3R2,** **02h: VSR2000-3R3,** **03h: VSR2000-3R5,** **04h ~ 0FFh: Reserved.**	**N/A**
8007	**1**	**RO**		**OTN Application Code**	**Any CFP module which supports an application which includes OTN and additional applications such as SONET/SDH, Ethernet, Fibre channel or other, shall record the value in OTN Application Code as follows.** **00h: Undefined type,** **01h: VSR2000-3R2F,** **02h: VSR2000-3R3F,** **03h: VSR2000-3R5F,** **04h: VSR2000-3L2F,** **05h: VSR2000-3L3F,** **06h: VSR2000-3L5F,** **07h: C4S1-2D1 (OTL3.4),** **08h: 4I1-9D1F (OTL4.4),** **09h: P1I1-3D1 (NRZ 40G 1300nm, 10km),** **0Ah: 4L1-9C1F (ITU OTU-4,40km,OTL4.4)** **0Bh: C4S1-2D1 of G.695,** **0Ch: ~ FFh: Reserved.**	**N/A**
8008	**1**	**RO**		**Additional Capable Rates Supported**	**Additional application rates module supporting.**	**N/A**
			7	Reserved		0
			6	OTU4 with Enhanced FEC	0: Not supported, 1: Supported.	N/A
			5	OTU3 with Enhanced FEC	0: Not supported, 1: Supported.	N/A
			4	111.8 Gbps	0: Not supported, 1: Supported.	N/A
			3	103.125 Gbps	0: Not supported, 1: Supported.	N/A
			2	41.25 Gbps	0: Not supported, 1: Supported.	N/A
			1	43 Gbps	0: Not supported, 1: Supported.	N/A
			0	39.8 Gbps	0: Not supported, 1: Supported.	N/A
8009	**1**	**RO**		**Number of Lanes Supported**	**Number of Network Lane supported and number of Host Lane supported in this particular module.**	**N/A**
			7~4	Number of Network Lanes	The value of 0 represents 16 network lanes supported. The values of 1 through 15 represent the actual number of network lanes supported.	N/A
			3~0	Number of Host Lanes	The value of 0 represents 16 host lanes supported. The values of 1 through 15 represent the actual number of host lanes supported.	N/A
800A	**1**	**RO**		**Media Properties**		**N/A**

CFP NVR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***LSB Unit***
			7~6	Media Type	00b: SMF , 01b: MMF (OM3, OM4), 10b: Reserved, 11b: Copper.	N/A
			5	Directionality	0: Normal, 1: BiDi.	N/A
			4	Optical Multiplexing and De-multiplexing	0: Without optical MUX/DEMUX, 1: With optical MUX/DEMUX.	N/A
			3~0	Active Fiber per Connector	A 4-bit unsigned number representing number of active fibers for TX and RX per connector. For example, a CFP module supporting the 100GBASE-SR10 application using an MPO connector shall report 10 in Active Fiber per Connector. 0: 16 TX Lanes and 16 RX Lanes, 1: 1 TX Lane and 1 RX Lane, 4: 4 TX Lanes and 4 RX Lanes, 10: 10 TX Lanes and 10 RX Lanes, 12: 12 TX Lanes and 12 RX Lanes.	N/A
800B	**1**	**RO**	**7~0**	**Maximum Network Lane Bit Rate**	**8-bit value x 0.2 Gbps. It shall identify maximum data rate supported per network lane. For more complex modulation schemes than OOK (on/off keying), the value reported shall be the bit rate and not the baud rate. The value shall be based upon units of 0.2 Gbps. A value of 0h is considered undefined.** **The above description is not applicable to MSA-100GLH modules. See 8184h.**	**0.2 Gbps**
800C	**1**	**RO**	**7~0**	**Maximum Host Lane Bit Rate**	**8-bit value x 0.2 Gbps. It shall identify maximum data rate supported per host lane. The value shall be based upon units of 0.2 Gbps.**	**0.2 Gbps**
800D	**1**	**RO**	**7~0**	**Maximum Single Mode Optical Fiber Length**	**8-bit value x 1 km for single mode fiber length. For applications which operate over compensated transmission systems, it is suggested to enter an undefined value. A value of 0h is considered undefined.**	**1 km**
800E	**1**	**RO**	**7~0**	**Maximum Multi-Mode Optical Fiber Length**	**8-bit value x 10 m for multi-mode fiber length. It shall identify the specified maximum reach supported by the application for transmission over OM3 multi-mode fiber. The value shall be based upon units of 10 m. A value of 0h is considered undefined. [2.2] Use register 8181h for OM4 Maximum MMF Length**	**10 m**
800F	**1**	**RO**	**7~0**	**Maximum Copper Cable Length**	**8-bit value x 1 m for copper cable length. A value of 0h is considered undefined.**	**1 m**
8010	**1**	**RO**		**Transmitter Spectral Characteristics 1**		**N/A**
			7~5	Reserved		0
			4~0	Number of Active Transmit Fibers	A 4-bit value identifying the number of active optical fiber outputs supported. 0: 0 active transmit fiber (receive only), copper or undefined. 1~31: actual numbers of active transmit fiber.	N/A
8011	**1**	**RO**		**Transmitter Spectral Characteristics 2**		**N/A**
			7~5	Reserved		0
			4~0	Number of Wavelengths per active Transmit Fiber	A 4-bit value representing the number of wavelengths per active transmitting fiber. 0: An 850 nm MM source or undefined, 1~31: Actual number of wavelength per transmit fiber. For example, the value for 100GBASE-LR4 is 4.	N/A
8012	**2**	**RO**	**7~0**	**Minimum Wavelength per Active Fiber**	**16-bit unsigned value x 25 pm. (MSB is at 8012h, LSB is at 8013h). A value of 0 indicates a multimode source or undefined.**	**25 pm**
8014	**2**	**RO**	**7~0**	**Maximum Wavelength per Active**	**16-bit unsigned value x 25 pm. (MSB is at 8014h, LSB**	**25**

CFP NVR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***LSB Unit***
				Fiber	**is at 8015h). A value of 0 indicates a multimode source or undefined.**	**pm**
8016	**2**	**RO**	**7~0**	**Maximum per Lane Optical Width**	**Guaranteed range of laser wavelength. 16-bit unsigned value x 1 pm. MSB is at 8016h, LSB is at 8017h. For an example, the value for 100GBASE-LR4 with a maximum specified optical wavelength width of 2.1nm for network lane L_3 would be 834h. A value of 0 indicates a multimode source or undefined.**	**1 pm**
8018	**1**	**RO**		**Device Technology 1**		**N/A**
			7~4	Laser Source Technology	A 4-bit value coding laser (or transmitter) technology used in a module. 0000b: VCSEL, 0001b: FP, 0010b: DFB, 0011b: DBR, 0100b: Copper, 0101b: External Cavity, 0110b ~ 1111b:Reserved.	N/A
			3~0	Transmitter modulation technology	A 4-bit value coding modulator technology used in a module. 0000b: DML, 0001b: EML, 0010b: InP-MZ, 0011b: LN-MZ 0100b: Copper, 0101b ~ 1111b: Reserved.	N/A
8019	**1**	**RO**		**Device Technology 2**		**N/A**
			7	Wavelength control	0: No wavelength control, 1: Active wavelength control.	N/A
			6	Cooled transmitter	0: Un-cooled transmitter device, 1: Cooled or Semi-cooled transmitter.	N/A
			5	Tunability	0: Transmitter not Tunable, 1: Transmitter Tunable.	N/A
			4	VOA implemented	0: Detector side VOA not implement, 1: Detector side VOA implement.	N/A
			3~2	Detector Type	00b: Undefined, (Use for Coherent type) 01b: PIN detector, 10b: APD detector, 11b: Optical Amplifier + PIN detector.	N/A
			1	CDR with EDC	0: CDR without EDC, 1: CDR with EDC.	N/A
			0	Reserved		0
801A	**1**	**RO**		**Signal Code**		**N/A**
			7~6	Modulation	00b: Undefined, 01b: NRZ, 10b: RZ, 11b: Reserved.	N/A
			5~2	Signal coding	0000b: Non-PSK, 0001b: ODB, 0010b: DPSK, 0011b: QPSK, 0100b: DQPSK, 0101b: DPQPSK, 0110~1010b: Reserved, 1011b: 16QAM, 1100b: 64QAM, 1101b: 256QAM, 1110~1111b: Reserved.	N/A
			1~0	Reserved		0
801B	**1**	**RO**	**7~0**	**Maximum Total Optical Output Power per Connector**	**Unsigned 8 bit value * 100 uW. Value 0 = undefined.**	**100 uW**

CFP NVR 1						
Hex Addr	*Size*	*Access Type*	*Bit*	*Register Name* *Bit Field Name*	*Description*	*LSB Unit*
801C	**1**	**RO**	**7~0**	**Maximum Optical Input Power per Network Lane**	**Unsigned 8 bit value * 100 uW. Value 0 = undefined.**	**100 uW**
801D	**1**	**RO**	**7~0**	**Maximum Power Consumption**	**Unsigned 8 bit value * 200 mW. Value 0 = undefined. These bits are only applicable to CFP Modules. They are not applicable to MSA-100GLH modules. See 0x8186h.**	**200 mW**
801E	**1**	**RO**	**7~0**	**Maximum Power Consumption in Low Power Mode**	**Unsigned 8 bit value * 20 mW. Value 0 = undefined. These bits are only applicable to CFP Modules. They are not applicable to MSA-100GLH modules. See 0x8188h.**	**20 mW**
801F	**1**	**RO**	**7~0**	**Maximum Operating Case Temp Range**	**Signed 8 bit value of 1 degC with valid range from -127 to +127 degC. Use 2's complement representation. Value of -128 indicates undefined.**	**1 deg C**
8020	**1**	**RO**	**7~0**	**Minimum Operating Case Temp Range**	**Signed 8 bit value of 1 degC with valid range from –127 to +127 degC. Use 2's complement representation. Value of -128 indicates undefined.**	**1 deg C**
8021	**16**	**RO**	**7~0**	**Vendor Name**	**Vendor (manufacturer) name in any combination of letters and/or digits in ASCII code, left aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name or the stock exchange code for the corporation. Vendor is the CFP module vendor.**	**N/A**
8031	**3**	**RO**	**7~0**	**Vendor OUI**	**The vendor organizationally unique identifier field (vendor OUI) is a 3-byte field that contains the IEEE Company Identifier for the vendor. The OUI format is defined by IEEE 802, section 9.1, which specifies "a string of three octets, using the hexadecimal representation", which lists the OUI bytes in forward order. For example, ABCDEFh will have ABh stored in register 8031h, CDh in register 8032h, and EFh in register 8033h.**	**N/A**
8034	**16**	**RO**	**7~0**	**Vendor Part Number**	**Vendor (manufacturer) part number in any combination of letters and/or digits in ASCII code, left aligned and padded on the right with ASCII spaces (20h). All zero value means undefined. Vendor is the CFP module vendor.**	**N/A**
8044	**16**	**RO**	**7~0**	**Vendor Serial Number**	**Vendor (manufacturer) serial number in any combination of letters and/or digits in ASCII code, left aligned and padded on the right with ASCII spaces (20h). All zero means unfined.**	**N/A**
8054	**8**	**RO**	**7~0**	**Date Code**	**Vendor (manufacturer) date code in ASCII characters, in the format YYYYMMDD (e.g., 20090310 for March 10, 2009). One character at each MDIO address. 1st letter of above format is at smaller address.**	**N/A**
805C	**2**	**RO**	**7~0**	**Lot Code**	**A 2-byte value representing lot code in any combination of letters and/or digits in ASCII code.**	**N/A**
805E	**10**	**RO**	**7~0**	**CLEI Code**	**CLEI Code in any combination of letters and/or digits in ASCII code.**	**N/A**
8068	**1**	**RO**	**7~0**	**CFP MSA Hardware Specification Revision Number**	**This register indicates the CFP MSA Hardware Specification version number supported by the transceiver. The 8 bits are used to represent the version number times 10. This yields a max of 25.5 revisions.**	**N/A**
8069	**1**	**RO**	**7~0**	**CFP MSA Management Interface Specification Revision Number**	**This register indicates the CFP MSA Management Interface Specification version number supported by the transceiver. The 8 bits are used to represent the version number times 10. This yields a max of 25.5 revisions.**	
806A	**2**	**RO**	**7~0**	**Module Hardware Version Number**	**A two-register number in the format of x.y with x at lower address and y at higher address. All zero value indicates undefined.**	**N/A**

CFP NVR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***LSB Unit***
806C	**2**	**RO**	**7~0**	**Module Firmware Version Number**	**A two-register number in the format of x.y with x at lower address and y at higher address. All zero value indicates undefined.**	**N/A**
806E	**1**	**RO**		**Digital Diagnostic Monitoring Type**		**N/A**
			7~4	Reserved		0
			3	Received power measurement type	0: OMA, 1: Average Power.	N/A
			2	Transmitted power measurement type	0: OMA, 1: Average Power.	N/A
			1~0	Reserved		0
806F	**1**	**RO**		**Digital Diagnostic Monitoring Capability 1**	**Module level DDM capability.**	**N/A**
			7~6	Transceiver auxiliary monitor 2	00b: Not supported, 01b ~ 11b: TBD.	N/A
			5~4	Transceiver auxiliary monitor 1	00b: Not supported, 01b ~ 11b: TBD.	N/A
			3	Reserved		0
			2	Transceiver SOA bias current monitor	0: Not supported, 1: supported.	N/A
			1	Transceiver power supply voltage monitor	0: Not supported, 1: supported.	N/A
			0	Transceiver temperature monitor	Detailed definition is provided by vendor. 0: Not supported, 1: supported.	N/A
8070	**1**	**RO**		**Digital Diagnostic Monitoring Capability 2**	**Per lane DDM capability.**	**N/A**
			7~4	Reserved		0
			3	Network Lane received power monitor	0: Not supported, 1: supported.	N/A
			2	Network Lane laser output power monitor	0: Not supported, 1: supported.	N/A
			1	Network Lane laser bias current monitor	0: Not supported, 1: supported.	N/A
			0	Network Lane laser temperature monitor	0: Not supported, 1: supported.	N/A
8071	**1**	**RO**		**Module Enhanced Options**		**N/A**
			7	Host Lane Loop-back	0: Not supported, 1: Supported.	N/A
			6	Host Lane PRBS Supported	0: Not supported, 1: Supported.	N/A
			5	Host Lane emphasis control	0: Not supported, 1: Supported.	N/A
			4	Network Lane Loop-back	0: Not Supported 1: Supported	N/A
			3	Network Lane PRBS	0: Not Supported 1: Supported	N/A
			2	Decision Threshold control function of FEC	This bit indicates whether Amplitude Adjustment function is supported in A280h~A28Fh or B300h~B30Fh 0: Not Supported 1: Supported	N/A
			1	Decision Phase control function of FEC	This bit indicates whether Phase Adjustment function is supported in A280h ~ A28Fh or B300h~B30Fh. 0: Not supported, 1: Supported.	N/A
			0	Unidirectional TX/RX only Operation Modes	0: Not supported, 1: Supported.	N/A
8072	**1**	**RO**	**7~0**	**Maximum High-Power-up Time**	**Fully power up time required by module. Unsigned 8-bit value * 1 sec. Use 1 sec if the actual time is less than 1 sec.**	**1 sec**
8073	**1**	**RO**	**7~0**	**Maximum TX-Turn-on Time**	**Maximum time required to turn on all TX lanes and to let them reach stability. Unsigned 8-bit value * 1 sec. Use 1 sec if it is less than 1 sec.**	**1 sec.**
8074	**1**	**RO**	**7~0**	**Host Lane Signal Spec**	**00h: Unspecified, 01h: CAUI, 02h: XLAUI, 03h: SFI5.2, 04h: SFI-S, 05h: OTL3.4, 06h: OTL4.10, 07h: OTL4.4, 08h: STL256.4, 09h: CPPI,**	**N/A**

CFP NVR 1								
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***			***LSB Unit***
					0Ah: CAUI-4, 0Bh: CAUI-4f, 0Ch: CEI-28G VSR, 0Dh: MLG1.0, 0Eh: MLG1.1 0Fh: MLG2.0, 0Ch-FEh: Reserved. FFh: Multiple Modes Supported (see registers 81C0~81C7 for supported modes).			
8075	**1**	**RO**		**Heat Sink Type**				**N/A**
			7~1	Reserved				0
			0	Heat Sink Type	0: Flat top, 1: Integrated heat sink.			N/A
8076	**1**	**RO**	**7~0**	**Maximum TX-Turn-off Time**	**Maximum time required to transit the "TX-Turn-off" state. The host may use this value as the time-out value. Unsigned 8-bit value * 1 ms.**			**1 ms**
8077	**1**	**RO**	**7~0**	**Maximum High-Power-down Time**	**Maximum time required from entering the "High-Power-down" state to exit from this state. Unsigned 8-bit value * 1 sec. Use 1 sec if it is less than 1 second.**			**1 sec.**
8078	**1**	**RO**		**Module Enhanced Options 2**				**N/A**
			7~6	Reserved				N/A
			5	Host Lane Equalization control function	0: Not supported, 1: Supported.			N/A
			4	Active Decision Voltage and Phase Function	0: Not supported, 1: Supported.			N/A
			3	RX FIFO Reset	0: Not supported, 1: Supported.			N/A
			2	RX FIFO Auto Reset	0: Not supported, 1: Supported.			N/A
			1	TX FIFO Reset	0: Not supported, 1: Supported.			N/A
			0	TX FIFO Auto Reset	0: Not supported, 1: Supported.			N/A
8079	**1**	**RO**		**Transmitter Monitor Clock Options**	**The CFP module may supply an optional transmitter monitor clock. This clock is intended to be used as a reference for measurements of the optical input. If provided, the clock shall operate at a faction of either host lane rate or a network lane rate. A module may support multiple options. For the below bit values, 0 = not supported, 1 = supported.**			**0**
					CFP or CFP2 10x10 mode	CFP2 4x25 mode or CFP4	Of Source Lane	
			7	TX MCLK Option 7	1/16	1/40	Host	0
			6	TX MCLK Option 6	1/16		Network	0
			5	TX MCLK Option 5	1/64	1/160	Host	0
			4	TX MCLK Option 4	1/64	-	Network	0
			3	Reserved	-	-	Host	0
			2	TX MCLK Option 2	1/8	1/8	Network	0
			1	TX MCLK Option 1	-	1/32	Host	0
			0	TX MCLK Option Support	Indicating whether this option is supported or not. 0: Not supported, 1: Supported.			0
807A	**1**	**RO**		**Receiver Monitor Clock Options**	**The CFP module may supply an optional receiver monitor clock. This clock is intended to be used as a reference for measurements of the optical input. If provided, the clock shall operate at a faction of either host lane rate or a network lane rate. A module may support multiple options. For the below bit values, 0 = not supported, 1 = supported.**			**0**
					CFP or CFP2 10x10 mode	CFP2 4x25 mode or CFP4	Of Source Lane	
			7	RX MCLK Option 7	1/16	1/40	Host	0
			6	RX MCLK Option 6	1/16		Network	0
			5	RX MCLK Option 5	1/64	1/160	Host	0
			4	RX MCLK Option 4	1/64	-	Network	0

<table>
<tr><th colspan="11">CFP NVR 1</th></tr>
<tr><th>Hex Addr</th><th>Size</th><th>Access Type</th><th>Bit</th><th>Register Name
Bit Field Name</th><th colspan="5">Description</th><th>LSB Unit</th></tr>
<tr><td></td><td></td><td></td><td>3</td><td>Reserved</td><td>-</td><td colspan="2">-</td><td colspan="2">Host</td><td>0</td></tr>
<tr><td></td><td></td><td></td><td>2</td><td>RX MCLK Option 2</td><td>1/8</td><td colspan="2">-</td><td colspan="2">Network</td><td>0</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>RX MCLK Option 1</td><td>-</td><td colspan="2">1/32</td><td colspan="2">Host</td><td>0</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>RX MCLK Option Support</td><td colspan="5">Indicating whether this option is supported or not. 0=not supported, 1=Supported.</td><td>0</td></tr>
<tr><td>807B [2.0]</td><td>2</td><td>RO</td><td>7~0</td><td>Module Firmware B Version Number</td><td colspan="5">A two-register number in the format of x.y with x at lower address and y at higher address.</td><td>N/A</td></tr>
<tr><td>807D [2.2]</td><td>1</td><td>RO</td><td>7~0</td><td>Maximum MDIO Ready Time</td><td colspan="5">An 8-bit unsigned number representing Maximum MDIO Ready Time due to module software upgrade introduced MDIO down time in seconds.</td><td>Sec.</td></tr>
<tr><td>807E [2.2]</td><td>1</td><td>RO</td><td></td><td>CFP and CFP2/4 Extended Identifier</td><td colspan="5"></td><td></td></tr>
<tr><td></td><td></td><td></td><td>7~6</td><td>Extended Power Class</td><td colspan="5">This field defines coding extended power classes for CFP, CFP2, CFP4, used together with register 8001h. For CFP2 modules if power class > 3, see Section 4.1.1.2.1 for recommended power up sequence.</td><td>N/A</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>Bits 1~0 Value</td><td>Power Class</td><td>CFP</td><td>CFP2</td><td>CFP4</td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>00b</td><td>4</td><td>≤ 32 W</td><td>≤ 12 W</td><td>≤ 6 W</td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>01b</td><td>5</td><td>≤ 40 W</td><td>≤ 15 W</td><td>≤ 7.5 W</td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>10b</td><td>6</td><td>≤ 48 W</td><td>≤ 18 W</td><td>≤ 9 W</td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>11b</td><td>N/A</td><td>NA</td><td>NA</td><td>NA</td><td></td></tr>
<tr><td></td><td></td><td></td><td>5</td><td>MDIO Port Address Scheme Configuration</td><td colspan="5">1-bit field specifies two MDIO Port Address modes (See Section 2.1.1 for additional information).
0: CFP2 only multi-device Type functionality scheme is used;
1: CFP/CFP2/CFP4 Common MDIO Port Address scheme with effective port address rage from 0 to 31.</td><td>N/A</td></tr>
<tr><td></td><td></td><td></td><td>4~0</td><td>Reserved</td><td colspan="5"></td><td>0</td></tr>
<tr><td>807F</td><td>1</td><td>RO</td><td>7~0</td><td>CFP NVR 1 Checksum</td><td colspan="5">The 8-bit unsigned sum of all CFP NVR 1 contents from address 8000h through 807Eh inclusive.</td><td>N/A</td></tr>
</table>

5.2 CFP NVR 2 Table: Alarm/Warning Threshold Registers

This whole table contains alarm and warning thresholds for DDM A/D measurement values, listed in CFP registers 8080h through 80F6h. Each register field is a 16-bit value with the type of signed and unsigned detailed in *Table 24 CFP NVR 2*. Each register field uses two addresses with MSB at lower address.

Each A/D value has a corresponding high alarm, low alarm, high warning and low warning threshold. The warning thresholds have more conservative value in terms of reporting the monitored A/D measurements while alarm thresholds represent more severe conditions that call for immediate attention when A/D measurements hit these values. These factory-set values allow the host to determine when a particular value is outside of “normal” limits as determined by the CFP module manufacturer. It is assumed that these threshold values will vary with different technologies and different implementations.

Table 24 CFP NVR 2

CFP NVR 2						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***LSB Unit***
Alarm/Warning Threshold Registers						
8080	**2**	**RO**	**7~0**	**Transceiver Temp High Alarm Threshold**	**These thresholds are a signed 16-bit integer with LSB = 1/256 of a degree Celsius representing a range from -128 to + 127 255/256 degree C. MSA valid range is between –40 and +125C." MSB stored at low address, LSB stored at high address.**	**1/256 degC**
8082	**2**	**RO**	**7~0**	**Transceiver Temp High Warning Threshold**		
8084	**2**	**RO**	**7~0**	**Transceiver Temp Low Warning Threshold**		
8086	**2**	**RO**	**7~0**	**Transceiver Temp Low Alarm Threshold**		
8088	**2**	**RO**	**7~0**	**VCC High Alarm Threshold**	**These thresholds are an unsigned 16-bit integer with LSB = 0.1 mV, representing a range of voltage from 0 to 6.5535 V. MSB stored at low address, LSB stored at high address.** **If Module Identifier (8000h) = 10h (168-pin 5x7 MSA 100GLH), then scale LSB = 1mV.**	**0.1 mV**
808A	**2**	**RO**	**7~0**	**VCC High Warning Threshold**		
808C	**2**	**RO**	**7~0**	**VCC Low Warning Threshold**		
808E	**2**	**RO**	**7~0**	**VCC Low Alarm Threshold**		
8090	**2**	**RO**	**7~0**	**SOA Bias Current High Alarm Threshold**	**These threshold values are an unsigned 16-bit integer with LSB = 2 uA, representing a range of current from 0 to 131.072 mA. MSB stored at low address, LSB stored at high address.**	**2 uA**
8092	**2**	**RO**	**7~0**	**SOA Bias Current High Warning Threshold**		
8094	**2**	**RO**	**7~0**	**SOA Bias Current Low Warning Threshold**		
8096	**2**	**RO**	**7~0**	**SOA Bias Current Low Alarm Threshold**		
8098	**2**	**RO**	**7~0**	**Auxiliary 1 Monitor High Alarm Threshold**	**TBD**	**TBD**
809A	**2**	**RO**	**7~0**	**Auxiliary 1 Monitor High Warning Threshold**	**TBD**	
809C	**2**	**RO**	**7~0**	**Auxiliary 1 Monitor Low Warning Threshold**	**TBD**	
809E	**2**	**RO**	**7~0**	**Auxiliary 1 Monitor Low Alarm Threshold**	**TBD**	
80A0	**2**	**RO**	**7~0**	**Auxiliary 2 Monitor High Alarm Threshold**	**TBD**	**TBD**
80A2	**2**	**RO**	**7~0**	**Auxiliary 2 Monitor High Warning Threshold**	**TBD**	
80A4	**2**	**RO**	**7~0**	**Auxiliary 2 Monitor Low Warning Threshold**	**TBD**	
80A6	**2**	**RO**	**7~0**	**Auxiliary 2 Monitor Low Alarm Threshold**	**TBD**	
80A8	**2**	**RO**	**7~0**	**Laser Bias Current High Alarm Threshold**	**Alarm and warning thresholds for measured laser bias current. Reference A2A0h Description for additional information. MSB stored at low address, LSB stored at high address.**	**See A2A 0h**
80AA	**2**	**RO**	**7~0**	**Laser Bias Current High Warning Threshold**		
80AC	**2**	**RO**	**7~0**	**Laser Bias Current Low Warning Threshold**		
80AE	**2**	**RO**	**7~0**	**Laser Bias Current Low Alarm Threshold**		
80B0	**2**	**RO**	**7~0**	**Laser Output Power High Alarm Threshold**	**Alarm and warning thresholds for measured laser output power. For additional information see A2B0h in case of CFP or B330 in case of 100GLH Module. MSB stored**	**See A2B 0h Or**
80B2	**2**	**RO**	**7~0**	**Laser Output Power High Warning Threshold**		

CFP NVR 2						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***LSB Unit***
80B4	**2**	**RO**	**7~0**	**Laser Output Power Low Warning Threshold**	**at low address, LSB stored at high address.**	**B330h**
80B6	**2**	**RO**	**7~0**	**Laser Output Power Low Alarm Threshold**		
80B8	**2**	**RO**	**7~0**	**Laser Temperature High Alarm Threshold**	**Alarm and warning thresholds for measured received input power. Reference A2C0h Description for additional information. MSB stored at low address, LSB stored at high address.**	**See A2C0h**
80BA	**2**	**RO**	**7~0**	**Laser Temperature High Warning Threshold**		
80BC	**2**	**RO**	**7~0**	**Laser Temperature Low Warning Threshold**		
80BE	**2**	**RO**	**7~0**	**Laser Temperature Low Alarm Threshold**		
80C0	**2**	**RO**	**7~0**	**Receive Optical Power High Alarm Threshold**	**Alarm and warning thresholds for measured received input power. Reference A2D0h Description for additional information. MSB stored at low address, LSB stored at high address.**	**See A2D0h**
80C2	**2**	**RO**	**7~0**	**Receive Optical Power High Warning Threshold**		
80C4	**2**	**RO**	**7~0**	**Receive Optical Power Low Warning Threshold**		
80C6	**2**	**RO**	**7~0**	**Receive Optical Power Low Alarm Threshold**		
80C8 [2.0]	**2**	**RO**	**7~0**	**RX Laser Bias Current High Alarm**	**Definition specified by module vendor. MSB stored at low address. LSB stored at high address.**	**TBD**
80CA [2.0]	**2**	**RO**	**7~0**	**RX Laser Bias Current High Warning**	**Definition specified by module vendor. MSB stored at low address. LSB stored at high address.**	**TBD**
80CC [2.0]	**2**	**RO**	**7~0**	**RX Laser Bias Current Low Warning**	**Definition specified by module vendor. MSB stored at low address. LSB stored at high address.**	**TBD**
80CE [2.0]	**2**	**RO**	**7~0**	**RX Laser Bias Current Low Alarm**	**Definition specified by module vendor. MSB stored at low address. LSB stored at high address.**	**TBD**
80D0 [2.0]	**2**	**RO**	**7~0**	**RX Laser Output Power High Alarm**	**Definition specified by module vendor. MSB stored at low address. LSB stored at high address.**	**TBD**
80D2 [2.0]	**2**	**RO**	**7~0**	**RX Laser Output Power High Warning**	**Definition specified by module vendor. MSB stored at low address. LSB stored at high address.**	**TBD**
80D4 [2.0]	**2**	**RO**	**7~0**	**RX Laser Output Power Low Warning**	**Definition specified by module vendor. MSB stored at low address. LSB stored at high address.**	**TBD**
80D6 [2.0]	**2**	**RO**	**7~0**	**Laser Output Power Low Alarm**	**Definition specified by module vendor. MSB stored at low address. LSB stored at high address.**	**TBD**
80D8 [2.0]	**2**	**R0**	**7~0**	**RX Laser Temperature High Alarm**	**Definition specified by module vendor. MSB stored at low address. LSB stored at high address.**	**TBD**
80DA [2.0]	**2**	**RO**	**7~0**	**RX Laser Temperature High Warning**	**Definition specified by module vendor. MSB stored at low address. LSB stored at high address.**	**TBD**
80DC [2.0]	**2**	**RO**	**7~0**	**RX Laser Temperature Low Warning**	**Definition specified by module vendor. MSB stored at low address. LSB stored at high address.**	**TBD**
80DE [2.0]	**2**	**RO**	**7~0**	**RX Laser Temperature Low Alarm**	**Definition specified by module vendor. MSB stored at low address. LSB stored at high address.**	**TBD**
80E0	**2**	**RO**	**7~0**	**TX Modulator Bias High Alarm**	**Definition specified by module vendor. MSB**	**TBD**

CFP NVR 2						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***LSB Unit***
[2.0]					**stored at low address. LSB stored at high address.**	
80E2 [2.0]	**2**	**RO**	**7~0**	**TX Modulator Bias High Warning**	**Definition specified by module vendor. MSB stored at low address. LSB stored at high address.**	**TBD**
80E4 [2.0]	**2**	**RO**	**7~0**	**TX Modulator Bias Low Warning**	**Definition specified by module vendor. MSB stored at low address. LSB stored at high address.**	**TBD**
80E6 [2.0]	**2**	**RO**	**7~0**	**TX Modulator Bias Low Alarm**	**Definition specified by module vendor. MSB stored at low address. LSB stored at high address.**	**TBD**
80E8 [2.2]	**2**	**RO**	**7~0**	**Host Configured Receive Optical Power High Alarm Permissible Minimum Threshold**	**MSB stored at low address, LSB stored at high address. 0000h indicates feature not supported and hence this range check is skipped.**	**NA**
80EA [2.2]	**2**	**RO**	**7~0**	**Host Configured Receive Optical Power High Warning Permissible Minimum Threshold**	**MSB stored at low address, LSB stored at high address. 0000h indicates feature not supported and hence this range check is skipped.**	**NA**
80EC [2.2]	**2**	**RO**	**7~0**	**Host Configured Receive Optical Power Low Warning Permissible Minimum Threshold**	**MSB stored at low address, LSB stored at high address. 0000h indicates feature not supported and hence this range check is skipped.**	**NA**
80EE [2.2]	**2**	**RO**	**7~0**	**Host Configured Receive Optical Power Low Alarm Permissible Minimum Threshold**	**MSB stored at low address, LSB stored at high address. 0000h indicates feature not supported and hence this range check is skipped.**	**NA**
80F0 [2.2]	**2**	**RO**	**7~0**	**Host Configured Receive Optical Power High Alarm Permissible Maximum Threshold**	**MSB stored at low address, LSB stored at high address. 0000h indicates feature not supported and hence this range check is skipped.**	**NA**
80F2 [2.2]	**2**	**RO**	**7~0**	**Host Configured Receive Optical Power High Warning Permissible Maximum Threshold**	**MSB stored at low address, LSB stored at high address. 0000h indicates feature not supported and hence this range check is skipped.**	**NA**
80F4 [2.2]	**2**	**RO**	**7~0**	**Host Configured Receive Optical Power Low Warning Permissible Maximum Threshold**	**MSB stored at low address, LSB stored at high address. 0000h indicates feature not supported and hence this range check is skipped.**	**NA**
80F6 [2.2]	**2**	**RO**	**7~0**	**Host Configured Receive Optical Power Low Alarm Permissible Maximum Threshold**	**MSB stored at low address, LSB stored at high address. 0000h indicates feature not supported and hence this range check is skipped.**	**NA**
80F8	**7**	**RO**	**7~0**	**Reserved**		**0**
80FF	**1**	**RO**	**7~0**	**CFP NVR 2 Checksum**	**The 8-bit unsigned sum of all CFP NVR 2 contents from address 8080h through 80FEh inclusive.**	**NA**

5.3 CFP NVR 3 Table: Network Lane BOL Measurement Registers

Table 25 CFP NVR 3 lists four beginning-of-life measurements of network lanes as the reference data for module aging consideration. CFP MSA specifies that vendor provides these data as an option. For details regarding each measurement please refer to description of each register in the table.

Table 25 CFP NVR 3

CFP NVR 3						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***LSB Unit***
				Network Lane BOL Measurements		
8100	**32**	**RO**	**7~0**	**RX Sensitivity Spec for network lanes 0 ~ 15.**	**RX Sensitivity measured in dBm @ BER=1e-12 at Typical condition. The value is a signed 16-bit integer with LSB = 0.01dBm. It uses two register addresses each for a total 32 register addresses for total 16 lanes.**	**0.01 dBm**
8120	**32**	**RO**	**7~0**	**TX Power Spec for network lanes 0 ~ 15.**	**TX Power measured in dBm at typical condition. The value is a signed 16-bit integer with LSB = 0.01dBm. It uses two register addresses each for a total 32 register addresses for total 16 lanes.**	**0.01 dBm**
8140	**32**	**RO**	**7~0**	**Measured ER for network lanes 0 ~ 15.**	**Measured Extinction ratio at Typical condition in dB. The value is an unsigned 16-bit integer with LSB = 0.01dB. It uses two register addresses each for a total 32 register addresses for total 16 lanes.**	**0.01 dB**
8160	**32**	**RO**	**7~0**	**Path Penalty for network lanes 0 ~ 15.**	**Path penalty @worst CD at Typical condition. The value is an unsigned 16-bit integer with LSB = 0.01dB. It uses two register addresses each for a total 32 register addresses for total 16 lanes.**	**0.01 dB**

5.4 CFP NVR 4 Table

The 0x8000h page Base ID Registers defined in *Table 26 CFP NVR 4* is designed to support CFP modules and MSA-100GLH modules with new registers added.

Table 26 CFP NVR 4 Miscellaneous Registers

CFP NVR 4						
Hex Add	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***LSB Unit***
8180	**1**	**RO**	**7~0**	**CFP NVR 3 Checksum**	**The 8-bit unsigned sum of all CFP NVR 3 contents from address 8100h through 817Fh inclusive.**	**N/A**
8181 [2.2]	**1**	**RO**	**7~0**	**Maximum OM4 Multi-Mode Optical Fiber Length**	**8-bit value x10 m specifying maximum length of OM4 multi-mode fiber. A value of 0h is considered undefined.**	**10 m**
8182 [2.0]	**2**	**RO**		**Extended Identifiers**	**MSB stored at low address. LSB stored at high address.**	
			15~2	Reserved		0
			1~0	Extended Power Class	00b: Power Class 4 Module (≤32W max); 01b: Power Class 5 Module (≤64W max); 10b: Power Class 6 Module (≤80W max); 11b: Reserved	00b
8184 [2.0]	**2**	**RO**	**15~0**	**Extended Maximum Network Lane Bit Rate**	**Unsigned 16-bit value x 0.1 Gbps. MSB stored at low address. LSB stored at high address.**	**N/A**
8186 [2.0]	**2**	**RO**	**15~0**	**Extended Maximum Power Consumption**	**Unsigned 16-bit value x 10 mW. MSB stored at low address. MSB stored at low address. LSB stored at high address.**	**N/A**
8188 [2.0]	**2**	**RO**	**15~0**	**Extended Maximum Power Consumption in Low Power**	**Unsigned 16-bit value x 1 mW. MSB stored at low address. LSB stored at high address.**	**N/A**

CFP NVR 4						
Hex Add	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***LSB Unit***
				Mode		
818A [2.0]	**2**	**RO**	**15~0**	**TX/RX Minimum Laser Frequency 1**	**An unsigned 16-bit integer with LSB = 1THz. MSB stored at low address. LSB stored at high address.**	**N/A**
818C [2.0]	**2**	**RO**	**15~0**	**TX/RX Minimum Laser Frequency 2**	**An unsigned 16-bit integer with LSB = 0.05 GHz. Value should not exceed 19999. MSB stored at low address. LSB stored at high address.**	**N/A**
818E [2.0]	**2**	**RO**	**15~0**	**TX/RX Maximum Laser Frequency 1**	**An unsigned 16-bit integer with LSB = 1THz. MSB stored at low address. LSB stored at high address.**	**N/A**
8190 [2.0]	**2**	**RO**	**15~0**	**TX/RX Maximum Laser Frequency 2**	**An unsigned 16-bit integer with LSB = 0.05 GHz. Value should not exceed 19999. MSB stored at low address. LSB stored at high address.**	**N/A**
8192 [2.0]	**2**	**RO**	**15~0**	**RX Laser Fine Tune Frequency Range (FTF) (Optional)**	**An unsigned 16-bit integer with LSB = 1 MHz. The range covers the min/max range symmetrically about 0. Set to zero if FTF is not supported. MSB stored at low address. LSB stored at high address.**	**0000h**
8194 [2.0]	**2**	**RO**	**15~0**	**TX Laser Fine Tune Frequency Range (FTF) (Optional)**	**An unsigned 16-bit integer with LSB = 1 MHz. The range covers the min/max range symmetrically about 0. Set to zero if FTF is not supported. MSB stored at low address. LSB stored at high address.**	**0000h**
8196 [2.0]	**2**	**RO**		**Laser Tuning Capabilities**	**MSB stored at low address. LSB stored at high address.**	
			15	6.25 GHz Grid Spacing	1 = Supported, 0 = Not Supported	N/A
			14	12.5 GHz Grid Spacing	1 = Supported, 0 = Not Supported	N/A
			13	25 GHz Grid Spacing	1 = Supported, 0 = Not Supported	N/A
			12	33 GHz Grid Spacing	1 = Supported, 0 = Not Supported	N/A
			11	50 GHz Grid Spacing	1 = Supported, 0 = Not Supported	N/A
			10	100 GHz Grid Spacing	1 = Supported, 0 = Not Supported	N/A
			9~0	Maximum Channels	Maximum channels supported based on minimum grid spacing supported	N/A
8198	**8**	**RO**	**7~0**	**Reserved**		
81A0 [2.2]	**8**	**RO**	**7~0**	**Network Lane n Vendor Specific Auxiliary 1 Monitor Thresholds**	**Definition provided by vendor, related to A340. For MSA 100GLH module, related to B140h.**	**0000h**
81A8 [2.2]	**8**	**RO**	**7~0**	**Network Lane n Vendor Specific Auxiliary 2 Monitor Thresholds**	**Definition provided by vendor, related to A350. For MSA 100GLH module, related to B150h.**	**0000h**
81B0 [2.2]	**8**	**RO**	**7~0**	**Network Lane n Vendor Specific Auxiliary 3 Monitor Threshold**	**Definition provided by vendor, related to A360. For MSA 100GLH module, related to B160h.**	**0000h**
81B8 [2.2]	**8**	**RO**	**7~0**	**Network Lane n Vendor Specific Auxiliary 4 Monitor Threshold**	**Definition provided by vendor, related to A370. For MSA 100GLH module, related to B170h.**	**0000h**
81C0 [2.2]	**6**	**RO**		**Reserved for Future Host Lane Signal Mode Bit Map Support**		**0000h**
81C6 [2.2]	**1**	**RO**		**Host Lane Signal Mode Bit Map 1**		**0000h**

CFP NVR 4						
Hex Add	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***LSB Unit***
			7~5	Reserved		
			4	OTL10.4	1: OTL10.4 supported, 0: OTL10.4 not supported	
			3	OTL3.4	1: OTL3.4 supported, 0: OTL3.4 not supported	
			2	OTL4.4	1: OTL4.4 supported, 0: OTL4.4 not supported	0
			1	MLG2.0	1: MLG2.0 supported, 0: MLG2.0 not supported	0
			0	MLG1.1	1: MLG1.1 supported, 0: MLG1.1 not supported	0
81C7 [2.2]	**1**	**RO**		**Host Lane Signal Mode Bit Map 0**		**0000h**
			7	MLG1.0	1: MLG1.0 supported, 0: MLG1.0 not supported.	0
			6	CPPI	1: CPPI supported, 0: CPPI not supported	0
			5	CEI-28G VSR	1: CEI-28G VSR supported, 0: CEI-28G VSR not supported	0
			4	CAUI-4f	1: CAUI-4f supported, 0: CAUI-4f not supported	0
			3	CAUI-4	1: CAUI-4 supported, 0: CAUI-4 not supported	0
			2	SFI5.2	1: SFI5.2 supported, 0: SFI5.2 not supported	0
			1	XLAUI	1: XLAUI supported, 0: XLAUI not supported	0
			0	CAUI	1: CAUI supported, 0: CAUI not supported	0
81C8	**47**	**RO**		**Reserved**		**0**
81FF	**1**	**RO**	**7~0**	**CFP NVR 4 Checksum**	**The 8-bit unsigned sum of all CFP NVR 4 contents from address 8181h through 81FEh inclusive.**	**N/A**

5.5 <u>CFP Module VR 1 Table</u>

Table 27 CFP Module VR 1 lists all the registers in several distinctive groups in terms of their function. All of the registers in this table use 16-bit data format. The description of each register field consists of three parts. The "Description" column of this table provides some rudimentary information about each register. For more involved description, a dedicated section of discussion is presented in "CFP Control and Signaling Theory". The sections presented in this chapter, provides additional information whenever it is appropriate.

Some CFP Control, Status and DDM registers are application specific. CFP MSA intent is to define registers and addresses. CFP MSA-compliant modules shall not use the specified registers for alternate purposes.

CFP MSA-compliant modules need not support all application-specific A/D or status registers defined here. For example, a parallel optical transceiver for short reach application may not need APD power supply or TEC status support.

5.5.1 CFP Command/Setup Registers

This group includes 8 registers that host may use to control module behavior.

5.5.1.1 NVR Access Control (A004h)

This is a one address register with all the details documented in 4.10.

5.5.1.2 PRG_CNTLs Function Select (A005h, A006, A007h)

Each of these registers selects a control function for the programmable control pins. Refer to 4.11.2 Programmable Control Functions for PRG_CNTLs for details.

5.5.1.3 PRG_ALRMs Source Select (A008h, A009h, A00Ah)

Each of these registers selects an alarm source for the programmable alarm pins. Refer to 4.11.3 Programmable Alarm Sources for PRG_ALRMS for details.

5.5.1.4 Module Bi-/Uni- Directional Operating Mode Select (A00Bh)

CFP module users may seek special applications where the CFP module is used for single directional operation. In addition to the “Description” column of this CFP register more information is referenced to 4.4 Special Modes of Operation.

5.5.2 Module Control Registers (A010h~5A015h)

These registers provide both additional and alternative controls to hardware pins, programmable control pins and extended features and options in controlling the CFP module. More information is documented in the “Description” column of the individual registers.

5.5.3 Module State Register (A016h)

Module State register provides real time States of the module operation. Its use has been discussed in detail in 4.1 CFP Module States and Related Signals. Note that this register is part of the global alarm system.

5.5.4 Module Alarm Summary Registers (A018h, A019h, A01Ah, A01Bh)

This set of CFP registers enable the fast diagnosis of locating the origin of a FAWS condition for the Host in response to a global alarm interrupt request generated by GLB_ALRM. This set of CFP registers is at the top level of the global alarm aggregation hierarchy. Host can use this set of CFP registers as the top-level index for tracking down the origin of the interrupt request. For more details in using these registers please reference 4.6.

5.5.5 Module FAWS Registers (A01Dh, A01Eh, A01Fh, A020h)

This set of CFP registers is the main source of module status and alarm/warning conditions.

5.5.6 Module FAWS Latch Registers (A022h, A023h, A024h, A025h, A026h)

All the CFP registers in this group contain the latched version of Module Alarm/Status Registers described above. Global Alarm uses these latched bits to report to the Host as depicted by *Figure 10 Global Alarm Signal Aggregation*. All of the bits in these CFP registers are cleared upon the Host reading.

5.5.7 Module FAWS Enable Registers (A028h, A029h, A02Ah, A02Bh, A02Ch)

All the CFP registers in this group are the enable registers for Module Alarm/Status Register group (A01Dh, A01Eh, A01Fh, A020h). These CFP registers allow host to enable or disable any particular FAWS bits to contribute to GLB_ALRM. Optional features and not-supported functions will have their corresponding Enable bit(s) set to 0 by the CFP during the Initialize state.

5.5.8 Module Analog A/D Value Registers (A02Fh, A030h, A031h, A032h, A033h)

Three analog quantities, Module Temperature Monitor A/D Value, Module Power Supply 3.3 V Monitor A/D Value, and SOA Bias Current A/D Value, are supported by this group of registers. These monitoring quantities are at module level and non-network lane specific. Two additional auxiliary monitoring quantities are specified future use.

The values in these and all other A/D registers are automatically updated with maximum period of 100 ms for single network lane applications. If the number of network lane is greater than 1, the maximum update period shall be 50 * (N + 1) ms, where N denotes the number of network lanes supported in the application.

5.5.9 Module PRBS Registers (A038h, A039h)

These are Network Lane PRBS Data Bit Count and Host Lane PRBS Data Bit Count registers. For their use reference 4.9 Bit Error Rate Calculation and the register descriptions.

Table 27 CFP Module VR 1

CFP Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
Module Command/Setup Registers						
A000 [2.2]	**2**	**WO**	**15~0**	**Password Entry (Optional)**	**Password for module registers access control. Two word value. MSW is in the lower address. Reading these registers always returns FFFFh.**	**0000h 0000h**
A002 [2.2]	**2**	**WO**	**15~0**	**Password Change (Optional)**	**New password entry. Two word value. MSW is in the lower address. Reading these registers always returns FFFFh.**	**0000h 0000h**
A004	**1**			**NVR Access Control**	**User NVRs Restore/Save command. Refer to 4.10.2 for details.**	**0000h**
		RW	15~9	Reserved	**Vendor specific.**	0
		RO	8~6	Reserved		000b
		RW	5	User Restore and Save Command	0: Restore the User NVR section, 1: Save the User NVR section.	0
		RO	4	Reserved		0
		RO	3~2	Command Status	00b: Idle, 01b: Command completed successfully,	00b

CFP Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
					10b: Command in progress, 11b: Command failed.	
		RW	1~0	Extended Commands	00b~01b: Vendor specific. 10b: Save User Password. If bit 5 = 0, this command has no effect, 11b: Restore/Save the User NVRs.	00b
A005	**1**			**PRG_CNTL3 Function Select**	**Selects, and assigns, a control function to PRG_CNTL3.**	**0000h**
		RO	15~8	Reserved		00h
		RW	7~0	Function Select Code	This multi-function input is used as HW_IL_MSB during the Initialize State and it can be programmed to other functions afterward. 0: Assert/De-Assert of PRG_CNTL3 has no effect, 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL3. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL3 Control (A010h.12) uses an active high logic, that is, 1 = Assert (Reset). 2~255: Reserved.	00h
A006	**1**			**PRG_CNTL2 Function Select**	**Selects, and assigns, a control function to PRG_CNTL2.**	**0000h**
		RO	15~8	Reserved		00h
		RW	7~0	Function Select Code	This multi-function input is used as HW_IL_LSB during the Initialize State and it can be programmed to other functions afterward. 0: Assert/De-Assert of PRG_CNTL2 has no effect, 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL2. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL2 Control (A010h.11) uses an active high logic, that is, 1 = Assert (Reset). 2~255: Reserved.	00h
A007	**1**			**PRG_CNTL1 Function Select**	**Selects, and assigns, a control function to PRG_CNTL1.**	**0001h**
		RO	15~8	Reserved		00h
		RW	7~0	Function Select Code	0: Assert/De-Assert of PRG_CNTL1 has no effect, 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL1. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL1 Control (A010h.10) uses an active high logic, that is, 1 = Assert (Reset). TRXIC_RSTn is the CFP MSA default function for PRG_CNTL1. 2~255: Reserved.	01h
A008	**1**			**PRG_ALRM3 Source Select**	**Selects, and assigns, an alarm source for PRG_ALRM3.**	**0003h**
		RO	15~8	Reserved		00h
		RW	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON, 2: Ready State, 3: Fault State, MSA default setting, 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, 5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL, 6: RX_NETWORK_LOL, 7: TX_LOSF, 8: TX_HOST_LOL, 9: OOA, Out of alignment, (Only applicable to certain products. If not implemented in the module, Writing 9 to this register has no effect and the register shall retain the previous value. This is also true for Registers A009h and A00Ah). 10~255: Reserved.	03h

CFP Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
A009	**1**			**PRG_ALRM2 Source Select**	**Selects, and assigns, an alarm source for PRG_ALRM2.**	**0002h**
		RO	15~8	Reserved		00h
		RW	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON, 2: Ready State, MSA default setting, 3: Fault State, 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, 5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL, 6: RX_NETWORK_LOL, 7: TX_LOSF, 8: TX_HOST_LOL, 9: OOA, Out of alignment, refer to description of A008h for details, 10~255: Reserved.	02h
A00A	**1**			**PRG_ALRM1 Source Select**	**Selects, and assigns, an alarm source for PRG_ALRM1.**	**0001h**
		RO	15~8	Reserved		00h
		RW	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON, MSA default setting, 2: Ready State, 3: Fault State, 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, 5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL, 6: RX_NETWORK_LOL, 7: TX_LOSF, 8: TX_HOST_LOL, 9: OOA, Out of alignment, refer to description of A008h for details, 10~255: Reserved.	01h
A00B	**1**			**Module Bi-/Uni-Directional Operating Mode Select**		**0000h**
		RO	15~3	Reserved		0
		RW	2~0	Module Bi/uni-direction mode Select	000b: Normal bi-directional mode, 001b: Uni-direction TX only mode (optional), 010b: Uni-direction RX only mode (optional), 011b: Special bi-directional mode (optional), 100b~111b: Reserved.	000b
A00C	**4**	**RO**		**Reserved**		**0000h**
Module Control Registers						
A010	**1**			**Module General Control**		**0000h**
		RW/SC/LH	15	Soft Module Reset	Register bit for module reset function. Writing a 0 to this bit has no effect regardless it was 0 or 1 previously. 1: Module reset assert.	0
		RW	14	Soft Module Low Power	Register bit for module low power function. 1: Assert.	0
		RW	13	Soft TX Disable	Register bit for TX Disable function. 1: Assert.	0
		RW	12	Soft PRG_CNTL3 Control	Register bit for PRG_CNTL3 control function. 1: Assert.	0
		RW	11	Soft PRG_CNTL2 Control	Register bit for PRG_CNTL2 control function. 1: Assert.	0
		RW	10	Soft PRG_CNTL1 Control	Register bit for PRG_CNTL1 control function. 1: Assert.	0
		RW	9	Soft GLB_ALRM Test	Command bit for software forced test signal. When this bit is	0

<table>
<tr><th colspan="7">CFP Module VR 1</th></tr>
<tr><th>Hex Addr.</th><th>Size</th><th>Access Type</th><th>Bit</th><th>Register Name
Bit Field Name</th><th>Description</th><th>Init Value</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>asserted it generates GLB_ALRM signal.
1: Assert.</td><td></td></tr>
<tr><td></td><td></td><td>RO</td><td>8~6</td><td>Reserved</td><td></td><td>0</td></tr>
<tr><td></td><td></td><td>RO</td><td>5</td><td>TX_DIS Pin State</td><td>Logical state of the TX_DIS pin.
1: Assert.</td><td>0</td></tr>
<tr><td></td><td></td><td>RO</td><td>4</td><td>MOD_LOPWR Pin State</td><td>Logical state of the MOD_LOPWR pin.
1: Assert.</td><td>0</td></tr>
<tr><td></td><td></td><td>RO</td><td>3</td><td>PRG_CNTL3 Pin State</td><td>Logical state of the PRG_CNTL3 pin.
1: Assert.</td><td>0</td></tr>
<tr><td></td><td></td><td>RO</td><td>2</td><td>PRG_CNTL2 Pin State</td><td>Logical state of the PRG_CNTL2 pin.
1: Assert.</td><td>0</td></tr>
<tr><td></td><td></td><td>RO</td><td>1</td><td>PRG_CNTL1 Pin State</td><td>Logical state of the PRG_CNTL1 pin.
1: Assert.</td><td>0</td></tr>
<tr><td></td><td></td><td>RO</td><td>0</td><td>Reserved</td><td></td><td>0</td></tr>
<tr><td>A011</td><td>1</td><td></td><td></td><td>Network Lane TX Control</td><td>This control acts upon all the network lanes.</td><td>0200h</td></tr>
<tr><td></td><td></td><td>RO</td><td>15</td><td>Reserved</td><td></td><td>0</td></tr>
<tr><td></td><td></td><td>RW</td><td>14</td><td>TX PRBS Generator Enable</td><td>0: Normal operation, 1: PRBS mode. (Optional)</td><td>0</td></tr>
<tr><td></td><td></td><td>RW</td><td>13~12</td><td>TX PRBS Pattern</td><td>Standard Modes
(A015h.15 = 0)
00b:2^7,
01b:2^15,
10b:2^23,
11b:2^31,

Extended Modes
(A015h.15 = 1)
00b: 2^9,
01b: Reserved,
10b: Reserved,
11b: Reserved.</td><td>00b</td></tr>
<tr><td></td><td></td><td>RW</td><td>11</td><td>TX De-skew Enable</td><td>0:Normal, 1:Disable</td><td>0</td></tr>
<tr><td></td><td></td><td>RW</td><td>10</td><td>TX FIFO Reset</td><td>This bit affects both host and network side TX FIFOs.
0: Normal operation, 1: Reset (Optional).</td><td>0</td></tr>
<tr><td></td><td></td><td>RW</td><td>9</td><td>TX FIFO Auto Reset</td><td>This bit affects both host and network side TX FIFOs.
0: Not Auto Reset, 1: Auto Reset. (Optional).</td><td>1</td></tr>
<tr><td></td><td></td><td>RW</td><td>8</td><td>TX Reset</td><td>0: Normal operation, 1: Reset. Definition and implementation are vendor specific.</td><td>0</td></tr>
<tr><td></td><td></td><td>RW

[2.2]</td><td>7~5</td><td>TX MCLK Control</td><td>A 3-bit field coding the MCLK rate control.
<table>
<tr><td>Code</td><td>Source Lane</td><td>CFP or CFP2 10x10 mode*</td><td>CFP2 4x25 mode* and CFP4*</td></tr>
<tr><td>000b</td><td colspan="3">Function disabled</td></tr>
<tr><td>001b</td><td>Of network lane rate</td><td>Reserved</td><td>1/32</td></tr>
<tr><td>010b</td><td>Of network lane rate</td><td>1/8</td><td>1/8</td></tr>
<tr><td>011b</td><td>Of host lane rate</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>100b</td><td>Of network lane rate</td><td>1/64</td><td>Reserved</td></tr>
<tr><td>101b</td><td>Of host lane rate</td><td>1/64</td><td>1/160</td></tr>
<tr><td>110b</td><td>Of network lane rate</td><td>1/16</td><td>Reserved</td></tr>
<tr><td>111b</td><td>Of host lane rate</td><td>1/16</td><td>1/40</td></tr>
</table></td><td>000b</td></tr>
<tr><td></td><td></td><td>RO</td><td>4</td><td>Reserved</td><td></td><td>0b</td></tr>
<tr><td></td><td></td><td>RW</td><td>3~1</td><td>TX Rate Select (Host Side)</td><td>A 3-bit field codes RX rate select implemented for a module. The selected rate is module ID and number of host lane dependent. Registers 8000h and 8009h shall be referenced to determine what signal type at what rate is supported.
<table>
<tr><td>Code</td><td>CFP or CFP2 10x10</td><td>CFP2 4x25</td><td>CFP4*</td></tr>
</table></td><td>000b or 110b</td></tr>
</table>

<table>
<tr><th colspan="7">CFP Module VR 1</th></tr>
<tr><th>Hex Addr.</th><th>Size</th><th>Access Type</th><th>Bit</th><th>Register Name
Bit Field Name</th><th>Description</th><th>Init Value</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>
<table>
<tr><td></td><td>mode*</td><td>mode*</td><td></td></tr>
<tr><td></td><td colspan="3">Signal Type and Rate Selected</td></tr>
<tr><td>000b</td><td>GbE 10.31</td><td>GbE 25.8</td><td>GbE 25.8</td></tr>
<tr><td>001b</td><td>SDH 9.95</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>010b</td><td>OTU3 10.7</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>011b</td><td>OTU4 11.2</td><td>OTU4 28</td><td>OTU4 28</td></tr>
<tr><td>100b</td><td>OTU3e1 11.14</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>101b</td><td>OTU3e2 11.15</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>110b</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>111b</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td colspan="4">* See 8000h for module ID and 8009h for Number of Host Lanes</td></tr>
</table>
</td><td></td></tr>
<tr><td></td><td></td><td>RW</td><td>0</td><td>TX Reference CLK Rate Select</td><td>A 1-bit field codes TX Reference CLK rate select implemented for a module. The selected rate is module ID and number of host lane dependent. Registers 8000h and 8009h shall be referenced to determine what signal type at what rate is supported.
<table>
<tr><td>Code</td><td>CFP or CFP2 10x10 mode*</td><td>CFP2 4x25 mode*</td><td>CFP4*</td></tr>
<tr><td></td><td colspan="3">CLK Divider</td></tr>
<tr><td>0b</td><td>1/16</td><td>1/40</td><td>1/40</td></tr>
<tr><td>1b</td><td>1/64</td><td>1/160</td><td>1/160</td></tr>
<tr><td colspan="4">* See 8000h for module ID and 8009h for Number of Host Lanes</td></tr>
</table>
</td><td>1b</td></tr>
<tr><td>A012</td><td>1</td><td></td><td></td><td>Network Lane RX Control</td><td>This control acts upon all the network lanes.</td><td>0200h</td></tr>
<tr><td></td><td></td><td>RW</td><td>15</td><td>Active Decision Voltage and Phase function</td><td>This bit activates the active decision voltage and phase function in the module.
0: not active, 1: active. (Optional)</td><td>0b</td></tr>
<tr><td></td><td></td><td>RW</td><td>14</td><td>RX PRBS Checker Enable</td><td>0: Normal operation, 1: PRBS mode. (Optional)</td><td>0b</td></tr>
<tr><td></td><td></td><td>RW</td><td>13~12</td><td>RX PRBS Pattern</td><td>
<table>
<tr><td>Standard Modes
<u>(A015.14 = 0)</u>
00b:2^7,
01b:2^15,
10b:2^23,
11b:2^31,</td><td>Extended Modes
<u>(A015.14 = 1)</u>
00b: 2^9,
01b: Reserved,
10b: Reserved,
11b: Reserved.</td></tr>
</table>
</td><td>00b</td></tr>
<tr><td></td><td></td><td>RW</td><td>11</td><td>RX Lock RX_MCLK to Reference CLK</td><td>0: Normal operation, 1: Lock RX_MCLK to REFCLK.</td><td>0b</td></tr>
<tr><td></td><td></td><td>RW</td><td>10</td><td>Network Lane Loop-back</td><td>0: Normal operation, 1: Network lane loop-back. (Optional)</td><td>0b</td></tr>
<tr><td></td><td></td><td>RW</td><td>9</td><td>RX FIFO Auto Reset</td><td>0: Not auto reset, 1: Auto reset. (Optional).</td><td>1b</td></tr>
<tr><td></td><td></td><td>RW</td><td>8</td><td>RX Reset</td><td>0: Normal operation, 1: Reset. Definition and implementation are vendor specific.</td><td>0b</td></tr>
<tr><td></td><td></td><td>RW
[2.2]</td><td>7~5</td><td>RX MCLK Control (optional)</td><td>3-bit field coding the MCLK rate control.
<table>
<tr><th>Code</th><th>Description</th><th>CFP or CFP2 10x10 mode</th><th>CFP2 4x25 mode or CFP4</th></tr>
<tr><td>000b</td><td colspan="3">Function disabled</td></tr>
<tr><td>001b</td><td>Of network lane rate</td><td>Reserved</td><td>1/32</td></tr>
<tr><td>010b</td><td>Of network lane rate</td><td>1/8</td><td>1/8</td></tr>
<tr><td>011b</td><td>Of host lane rate</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>100b</td><td>Of network lane rate</td><td>1/64</td><td>Reserved</td></tr>
<tr><td>101b</td><td>Of host lane rate</td><td>1/64</td><td>1/160</td></tr>
<tr><td>110b</td><td>Of network lane rate</td><td>1/16</td><td>Reserved</td></tr>
<tr><td>111b</td><td>Of host lane rate</td><td>1/16</td><td>1/40</td></tr>
</table>
</td><td>000b</td></tr>
</table>

<table>
<tr><th colspan="7">CFP Module VR 1</th></tr>
<tr><th>Hex Addr.</th><th>Size</th><th>Access Type</th><th>Bit</th><th>Register Name
Bit Field Name</th><th>Description</th><th>Init Value</th></tr>
<tr><td></td><td></td><td>RW</td><td>4</td><td>RX FIFO Reset</td><td>0: Normal, 1: Reset. (Optional).</td><td>0b</td></tr>
<tr><td></td><td></td><td>RW</td><td>3~1</td><td>RX Rate Select (Host Side)</td><td>A 3-bit field codes RX rate select implemented for a module. The selected rate is module ID and number of host lane dependent. Registers 8000h and 8009h shall be referenced to determine what signal type at what rate is supported.
<table>
<tr><th>Code</th><th>CFP or CFP2 10x10 mode*</th><th>CFP2 4x25 mode*</th><th>CFP4*</th></tr>
<tr><td></td><td colspan="3">Signal Type and Rate Selected</td></tr>
<tr><td>000b</td><td>GbE 10.31</td><td>GbE 25.8</td><td>GbE 25.8</td></tr>
<tr><td>001b</td><td>SDH 9.95</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>010b</td><td>OTU3 10.7</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>011b</td><td>OTU4 11.2</td><td>OTU4 28</td><td>OTU4 28</td></tr>
<tr><td>100b</td><td>OTU3e1 11.14</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>101b</td><td>OTU3e2 11.15</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>110b</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>111b</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td colspan="4">* See 8000h for module ID and 8009h for Number of Host Lanes</td></tr>
</table></td><td>000b</td></tr>
<tr><td></td><td></td><td>RW</td><td>0</td><td>RX Reference CLK Rate Select</td><td>A 1-bit field codes RX Reference CLK rate select implemented for a module. The selected rate is module ID and number of host lane dependent. Registers 8000h and 8009h shall be referenced to determine what signal type at what rate is supported.
<table>
<tr><td>Code</td><td>CFP or CFP2 10x10 mode*</td><td>CFP2 4x25 mode*</td><td>CFP4*</td></tr>
<tr><td></td><td colspan="3">CLK Divider</td></tr>
<tr><td>0b</td><td>1/16</td><td>1/40</td><td>1/40</td></tr>
<tr><td>1b</td><td>1/64</td><td>1/160</td><td>1/160</td></tr>
<tr><td colspan="4">* See 8000h for module ID and 8009h for Number of Host Lanes</td></tr>
</table></td><td>1b</td></tr>
<tr><td>A013</td><td>1</td><td>RW</td><td></td><td>Individual Network Lane TX_DIS Control</td><td>This register acts upon individual network lanes. Note that toggling individual network lane TX disable bit does not change module state.</td><td>0000h</td></tr>
<tr><td></td><td></td><td></td><td>15~0</td><td>Lane 15~0 Disable</td><td>Bits 15~0 disable Lanes 15~0 respectively.
0: Normal, 1: Disable.</td><td>0</td></tr>
<tr><td>A014</td><td>1</td><td></td><td></td><td>Host Lane Control</td><td>This control acts upon all the host lanes.</td><td>0000h</td></tr>
<tr><td></td><td></td><td>RO</td><td>15</td><td>Reserved</td><td></td><td>0</td></tr>
<tr><td></td><td></td><td>RW</td><td>14</td><td>TX PRBS Checker Enable</td><td>0: Normal operation, 1: PRBS mode. (Optional)</td><td>0</td></tr>
<tr><td></td><td></td><td>RW
RW
RW</td><td>13
12
11</td><td>TX PRBS Pattern 2
TX PRBS Pattern 1
TX PRBS Pattern 0</td><td>000b:2^7, 100b:2^23,
001b: 2^9, 101b: reserved,
010b:2^15, 110b:2^31,
011b: reserved, 111b: reserved.</td><td>000b</td></tr>
<tr><td></td><td></td><td>RW</td><td>10</td><td>Host Lane Loop-back Enable</td><td>0: Normal operation, 1: Host lane loop-back. (Optional)</td><td>0</td></tr>
<tr><td></td><td></td><td>RO</td><td>9</td><td>Reserved</td><td></td><td>0</td></tr>
<tr><td></td><td></td><td>RO</td><td>8</td><td>Reserved</td><td></td><td>0</td></tr>
<tr><td></td><td></td><td>RW</td><td>7</td><td>RX PRBS Generator Enable</td><td>0: Normal operation, 1: PRBS mode. (Optional)</td><td>0</td></tr>
<tr><td></td><td></td><td>RW
RW</td><td>6
5</td><td>RX PRBS Pattern 2
RX PRBS Pattern 1</td><td>000b:2^7, 100b:2^23,
001b: 2^9, 101b: reserved,</td><td>000b</td></tr>
</table>

CFP Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
		RW	4	RX PRBS Pattern 0	010b:2^15, 110b:2^31, 011b: reserved, 111b: reserved.	
		RO	3~0	Reserved		0h
A015 [2.2]	**1**	**RW**		**Module General Control 2**	**This register collects added module general control functions for CFP MSA MIS V2.2**	**0000h**
			15	Enable Tx Network Lane PRBS Modes.	Enables standard or extended Tx Network Lane PRBS Modes in Register A011. 0: Enable standard modes, 1: Enable extended modes.	0
			14	Enable Rx Network Lane PRBS Modes.	Enables standard or extended Rx Network Lane PRBS Modes in Register A012. 0: Enable standard modes, 1: Enable extended modes.	0
			13~12	MCLK Selection (CFP4)	Selects the source of the MCLK for CFP4 modules. 00b: MCLK Off 01b: MCLK = TX_MCLK 10b: MCLK = RX_MCLK 11b: Reserved.	0
			11	Tx Lane Offset Enable	Optional feature to enable delaying Tx Lanes by 32 bytes to prevent frame alignment bytes from overlapping. 0: Disabled, 1: Enabled	0
			10	Rx Lane Offset Enable	Optional feature to enable delaying Rx Lanes by 32 bytes to prevent frame alignment bytes from overlapping. 0: Disabled, 1: Enabled	0
			9	RX Power Monitor Alarm/Warning Threshold Select	0: MSA default registers 80C0h~80C7h, 1: Host Configured Receive Optical Power Threshold registers A03Ch~A03Fh.	0
			8	Reserved		0
			7~0	Electrical Interface Format Select (Optional)	Host writes to select in which mode the module should operate. 00h: Unspecified, 01h: CAUI, 02h: XLAUI, 03h: SFI5.2, 04h: SFI-S, 05h: OTL3.4, 06h: OTL4.10, 07h: OTL4.4, 08h: STL256.4, 09h: CPPI, 0Ah: CAUI-4, 0Bh: CAUI-4f, 0Ch: CEI-28G VSR, 0Dh: MLG1.0, 0Eh: MLG1.1 0Fh: MLG2.0, 10h~FFh: Reserved	00h
Module State Register						
A016	**1**	**RO**		**Module State**	**CFP module state. Only a single bit set at any time.**	**0000h**
			15~9	Reserved		0
			8	High-Power-down State	1: Corresponding state is active. Word value = 0100h.	0
			7	TX-Turn-off State	1: Corresponding state is active. Word value = 0080h.	0
			6	Fault State	1: Corresponding state is active. Word value = 0040h. (Also referred to as MOD_FAULT)	0
			5	Ready State	1: Corresponding state is active. Word value = 0020h. (Also referred to as MOD_READY)	0
			4	TX-Turn-on State	1: Corresponding state is active. Word value = 0010h.	0

CFP Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
			3	TX-Off State	1: Corresponding state is active. Word value = 0008h.	0
			2	High-Power-up State	1: Corresponding state is active. Word value = 0004h.	0
			1	Low-Power State	1: Corresponding state is active. Word value = 0002h.	0
			0	Initialize State	1: Corresponding state is active. Word value = 0001h.	0
Module Alarm Summary Registers						
A017	**1**	**RO**		**Reserved**		**0000h**
A018	**1**	**RO**		**Global Alarm Summary**		
			15	GLB_ALRM Assertion Status	Internal status of global alarm output. 1: Asserted.	0
			14	Host Lane Fault and Status Summary	Logical OR of all the enabled bits of Host Lane Fault and Status Summary register.	0
			13	Network Lane Fault and Status Summary	Logical OR of all the bits in the Network Lane Fault and Status Summary register.	0
			12	Network Lane Alarm and Warning Summary	Logical OR of all the bits in the Network Lane Alarm and Warning Summary register.	0
			11	Module Alarm and Warning 2 Summary	Logical OR of all the enabled bits of Module Alarms and Warnings 2 Latch register.	0
			10	Module Alarm and Warning 1 Summary	Logical OR of all the enabled bits of Module Alarms and Warnings 1 Latch register.	0
			9	Module Fault Summary	Logical OR of all the enabled bits of Module Fault Status Latch register.	0
			8	Module General Status Summary	Logical OR of all the enabled bits of Module General Status Latch register.	0
			7	Module State Summary	Logical OR of all the enabled bits of Module State Latch register.	0
			6~5	Reserved		
			4	CDB Command Completed	Logic OR of both CDB Status, CDB Command Completed Successfully and CDB Command Failed.	0
			3 [2.2]	Vendor Specific FAWS	Logical OR of all the enabled bits of Vendor Specific FAWS Latch register.	0
			2~1	Reserved		0
			0	Soft GLB_ALRM Test Status	Soft GLB_ALRM Test bit Status.	0
A019	**1**	**RO**		**Network Lane Alarm and Warning Summary**	**Each bit is the logical OR of all enabled bits in each of Network Lane Alarm and Warning Latch registers.**	**0000h**
			15~0	Lane n Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane n Network Lane Alarm and Warning Register. 1 = Fault asserted. n ranges from 0 to 15.	0
A01A	**1**	**RO**		**Network Lane Fault and Status Summary**	**Each bit is the logical OR of all enabled bits in each of the Network Lane fault and Status Latch registers.**	**0000h**
			15~0	Lane n Fault and Status Summary	Logical OR of all enabled bits in Latched Lane n Network Lane Fault and Status Register. 1 = Fault asserted. Lane number n ranges from 0 to 15.	0
A01B	**1**	**RO**		**Host Lane Fault and Status Summary**	**Each bit is the logical OR of all enabled bits in each of the Host Lane fault and Status Latch registers**	**0000h**
			15~0	Lane n Fault and Status Summary	Logical OR of all enabled bits in Latched Lane n Host Lane Fault and Status Register. 1 = Fault asserted. Lane number n ranges from 0 to 15.	0
A01C	**1**	**RO**		**Reserved**		**0**
Module FAWS Registers						
A01D	**1**	**RO**		**Module General Status**		**0000h**

CFP Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
			15	Reserved		0
			14	Reserved		0
			13	HW_Interlock	Module internally generated status signal. (FAWS_TYPE_A) 0: If module power <= Host cooling capacity or if hardware Interlock is not used, 1: If module power > Host cooling capacity.	0
			12~11	Reserved		0
			10	Loss of REFCLK Input	Loss of reference clock input. It is an optional feature. (FAWS_TYPE_B). 0: Normal, 1: Loss of signal.	0
			9	TX_JITTER_PLL_LOL	TX jitter PLL loss of lock. It is an optional feature. (FAWS_TYPE_B). 0: Normal, 1: Loss of lock.	0
			8	TX_CMU_LOL	TX CMU loss of lock. It is the loss of lock indicator on the network side of the CMU. It is an optional feature. (FAWS_TYPE_B). 0: Normal, 1: Loss of lock.	0
			7	TX_LOSF	Transmitter Loss of Signal Functionality. Logic OR of all of Network Lanes TX_LOSF bits. PRG_ALRMx mappable. . (FAWS_TYPE_C, since the TX must be enabled). **Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal.** 0: all transmitter signals functional, 1: any transmitter signal not functional.	0
			6	TX_HOST_LOL	TX IC Lock Indicator. Logic OR of all host lane TX_LOL bits. PRG_ALRMx mappable. (FAWS_TYPE_B). **Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal.** 0: Locked, 1: Loss of lock.	0
			5	RX_LOS	Receiver Loss of Signal. Logic OR of all of network lane RX_LOS bits. (FAWS_TYPE_B). **Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal.** 0: No network lane RX_LOS bit asserted, 1: Any network lane RX_LOS bit asserted.	0
			4	RX_NETWORK_LOL	RX IC Lock Indicator. Logic OR of all network lane RX_LOL bits. PRG_ALRMx mappable. (FAWS_TYPE_B). **Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal.** 0: Locked, 1: Loss of lock.	0
			3	Out of Alignment	Host lane skew out of alignment indicator. Applicable only for some internal implementations. (FAWS_TYPE_B). 0: Normal, 1: Out of alignment.	0
			2	Reserved		0
			1	HIPWR_ON	Status bit representing the condition of module in high power status. FAWS Type is not applicable. 0: Module is not in high power on status, 1: Module is in high powered on status.	0
			0	Reserved		0
A01E	**1**	**RO**		**Module Fault Status**	**Module Fault Status bit pattern. Only fatal faults that are potentially harmful to the module can trigger the bits here. All the bits are 0: Normal; 1: fault detected. When any bit in this register is a '1', The Module State register will also be**	**0000h**

CFP Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
					set to the Fault State.	
			15	Reserved	Reserved for extension of "other faults" in case of all the bits used up in this register.	0
			14~7	Reserved		0
			6	PLD or Flash Initialization Fault	PLD, CPLD, or FPGA initialization fault. (FAWS_TYPE_A)	0
			5	Power Supply Fault	1: Power supply is out of range. (FAWS_TYPE_A)	0
			4~2	Reserved		000b
			1	CFP Checksum Fault	1: CFP Checksum failed. (FAWS_TYPE_A)	0
			0	Reserved		0
A01F	**1**	**RO**		**Module Alarms and Warnings 1**		**0000h**
			15~12	Reserved		0000b
			11	Mod Temp High Alarm	Mod temp high Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			10	Mod Temp High Warning	Mod temp high Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			9	Mod Temp Low Warning	Mod temp low Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			8	Mod Temp Low Alarm	Mod temp low Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			7	Mod Vcc High Alarm	Input Vcc high Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			6	Mod Vcc High Warning	Input Vcc high Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			5	Mod Vcc Low Warning	Input Vcc low Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			4	Mod Vcc Low Alarm	Input Vcc low Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			3	Mod SOA Bias High Alarm	SOA bias current high alarm. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
			2	Mod SOA Bias High Warning	SOA bias current high warning. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
			1	Mod SOA Bias Low Warning	SOA bias current low warning. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
			0	Mod SOA Bias Low Alarm	SOA bias current low alarm. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
A020	**1**	**RO**		**Module Alarms and Warnings 2**		**0000h**
			15~8	Reserved		0
			7	Mod Aux 1 High Alarm	Module aux ch 1 high alarm. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted..	0
			6	Mod Aux 1 High Warning	Module aux ch 1 high warning. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
			5	Mod Aux 1 Low Warning	Module aux ch 1 low warning. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
			4	Mod Aux 1 Low Alarm	Module aux ch 1 low alarm. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
			3	Mod Aux 2 High Alarm	Module aux ch 2 high alarm. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
			2	Mod Aux 2 High Warning	Module aux ch 2 high warning. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
			1	Mod Aux 2 Low Warning	Module aux ch 2 low warning. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
			0	Mod Aux 2 Low Alarm	Module aux ch 2 low alarm. (FAWS Type is vendor TBD)	0

CFP Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
					0: Normal, 1: Asserted.	
A021 [2.2]	**1**	**RO**		**Vendor Specific FAWS**	**(Optional) Vendor Specified Module Fault, Alarm, Warning and Status. Contents are specified by the vendor.**	**0000h**
Module FAWS Latch Registers						
A022	**1**			**Module State Latch**	**CFP module state Latch.**	**0000h**
		RO	15~9	Reserved		0
		RO/LH/COR	8	High-Power-down State Latch	1: Latched.	0
		RO/LH/COR	7	TX-Turn-off State Latch	1: Latched.	0
		RO/LH/COR	6	Fault State Latch	1: Latched.	0
		RO/LH/COR	5	Ready State Latch	1: Latched.	0
		RO/LH/COR	4	TX-Turn-on State Latch	1: Latched.	0
		RO/LH/COR	3	TX-Off State Latch	1: Latched.	0
		RO/LH/COR	2	High-Power-up State Latch	1: Latched.	0
		RO/LH/COR	1	Low-Power State Latch	1: Latched.	0
		RO/LH/COR	0	Initialize State Latch	1: Latched.	0
A023	**1**			**Module General Status Latch**		**0000h**
		RO	15	Reserved		0
		RO	14	Reserved		0
		RO/LH/COR	13	HW_Interlock Latch	1: Latched.	0
		RO	12~11	Reserved		0
		RO/LH/COR	10	Loss of REFCLK Input Latch	1: Latched.	0
		RO/LH/COR	9	TX_JITTER_PLL_LOL Latch	1: Latched.	0
		RO/LH/COR	8	TX_CMU_LOL Latch	1: Latched.	0
		RO/LH/COR	7	TX_LOSF Latch	1: Latched. **Note:** Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0
		RO/LH/COR	6	TX_HOST_LOL Latch	1: Latched. **Note:** Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0
		RO/LH/COR	5	RX_LOS Latch	1: Latched. **Note:** Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0
		RO/LH/COR	4	RX_NETWORK_LOL Latch	1: Latched. **Note:** Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0
		RO/LH/COR	3	Out of Alignment Latch	1: Latched.	0
		RO	2~0	Reserved		000b
A024	**1**			**Module Fault Status Latch**	**Module Fault Status latched bit pattern.**	**0000h**
		RO	15~7	Reserved		0
		RO/LH/COR	6	PLD or Flash Initialization Fault Latch	1: Latched.	0
		RO/LH/COR	5	Power Supply Fault Latch	1: Latched.	0
		RO	4~2	Reserved		000b

CFP Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
		RO/LH/COR	1	CFP Checksum Fault Latch	1: Latched.	0
		RO	0	Reserved		0
A025	**1**			**Module Alarms and Warnings 1 Latch**		**0000h**
		RO	15~12	Reserved		0000b
		RO/LH/COR	11	Mod Temp High Alarm Latch	1: Latched.	0
		RO/LH/COR	10	Mod Temp High Warning Latch	1: Latched.	0
		RO/LH/COR	9	Mod Temp Low Warning Latch	1: Latched.	0
		RO/LH/COR	8	Mod Temp Low Alarm Latch	1: Latched.	0
		RO/LH/COR	7	Mod Vcc High Alarm Latch	1: Latched.	0
		RO/LH/COR	6	Mod Vcc High Warning Latch	1: Latched.	0
		RO/LH/COR	5	Mod Vcc Low Warning Latch	1: Latched.	0
		RO/LH/COR	4	Mod Vcc Low Alarm Latch	1: Latched.	0
		RO/LH/COR	3	Mod SOA Bias High Alarm Latch	1: Latched.	0
		RO/LH/COR	2	Mod SOA Bias High Warning Latch	1: Latched.	0
		RO/LH/COR	1	Mod SOA Bias Low Warning Latch	1: Latched.	0
		RO/LH/COR	0	Mod SOA Bias Low Alarm Latch	1: Latched.	0
A026	**1**			**Module Alarms and Warnings 2 Latch**		0
		RO	15~8	Reserved		0
		RO/LH/COR	7	Mod Aux 1 High Alarm Latch	1: Latched.	0
		RO/LH/COR	6	Mod Aux 1 High Warning Latch	1: Latched.	0
		RO/LH/COR	5	Mod Aux 1 Low Warning Latch	1: Latched.	0
		RO/LH/COR	4	Mod Aux 1 Low Alarm Latch	1: Latched.	0
		RO/LH/COR	3	Mod Aux 2 High Alarm Latch	1: Latched.	0
		RO/LH/COR	2	Mod Aux 2 High Warning Latch	1: Latched.	0
		RO/LH/COR	1	Mod Aux 2 Low Warning Latch	1: Latched.	0
		RO/LH/COR	0	Mod Aux 2 Low Alarm Latch	1: Latched.	0
A027 [2.2]	**1**	**RO/LH/COR**		**Vendor Specific FAWS Latch**	**(Optional) Vendor Specified Module Fault, Alarm, Warning and Status Latch. Contents are specified by the vendor.**	**0000h**
Module FAWS Enable Registers						
A028	**1**			**Module State Enable**	**GLB_ALRM Enable register for Module State change. One bit for each state.**	**006Ah**
		RO	15~9	Reserved		0

CFP Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
		RW	8	High-Power-down State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	7	TX-Turn-off State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	6	Fault State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	1
		RW	5	Ready State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	1
		RW	4	TX-Turn-on State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	3	TX-Off State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	1
		RW	2	High-Power-up State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	1	Low-Power State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence)	1
		RO	0	Initialize State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
A029	**1**			**Module General Status Enable**	**1: Enable signal to assert GLB_ALRM. Bits 14~0 are AND'ed with corresponding bits in the Module General Status Latch register; the result is used to assert GLB_ALRM. Bit 15 is the master enable of GLB_ALRM and it is AND'ed with the output of the "OR" gate output in Global Alarm Signal Aggregation, Figure 10.**	**A7F8h**
		RW	15	GLB_ALRM Master Enable	1: Enable.	1
		RO	14	Reserved		0
		RW	13	HW_Interlock	1: Enable.	1
		RO	12~11	Reserved		0
		RW	10	Loss of REFCLK Input Enable	1: Enable.	1
		RW	9	TX_JITTER_PLL_LOL Enable	1: Enable.	1
		RW	8	TX_CMU_LOL Enable	1: Enable.	1
		RW	7	TX_LOSF Enable	1: Enable.	1
		RW	6	TX_HOST_LOL Enable	1: Enable.	1
		RW	5	RX_LOS Enable	1: Enable.	1
		RW	4	RX_NETWORK_LOL Enable	1: Enable.	1
		RW	3	Out of Alignment Enable	1. Enable.	1
		RO	2~0	Reserved		000b
A02A	**1**			**Module Fault Status Enable**	**These bits are AND'ed with corresponding bits in the Module Fault Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.**	**0062h**
		RO	15~7	Reserved		0
		RW	6	PLD or Flash Initialization Fault Enable	1: Enable.	1
		RW	5	Power Supply Fault Enable	1: Enable.	1
		RO	4~2	Reserved		000b
		RW	1	CFP Checksum Fault Enable	1: Enable.	1
		RO	0	Reserved		0

CFP Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
A02B	**1**			**Module Alarm and Warnings 1 Enable**	**These bits are AND'ed with corresponding bits in the Module Alarm and Warnings 1 Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.**	**0FFFh**
		RO	15~12	Reserved		0000b
		RW	11	Mod Temp Hi Alarm Enable	1: Enable.	1
			10	Mod Temp Hi Warn Enable	1: Enable.	1
			9	Mod Temp Low Warning Enable	1: Enable.	1
			8	Mod Temp Low Alarm Enable	1: Enable.	1
			7	Mod Vcc High Alarm Enable	1: Enable.	1
			6	Mod Vcc High Warning Enable	1: Enable.	1
			5	Mod Vcc Low Warning Enable	1: Enable.	1
			4	Mod Vcc Low Alarm Enable	1: Enable.	1
			3	Mod SOA Bias High Alarm Enable	1: Enable.	1
			2	Mod SOA Bias High Warning Enable	1: Enable.	1
			1	Mod SOA Bias Low Warning Enable	1: Enable.	1
			0	Mod SOA Bias Low Alarm Enable	1: Enable.	1
A02C	**1**			**Module Alarms and Warnings 2 Enable**	**These bits are AND'ed with corresponding bits in the Module Alarm and Warnings 2 Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.**	**00FFh**
		RO	15~8	Reserved		00h
		RW	7	Mod Aux 1 High Alarm Enable	1: Enable.	1
			6	Mod Aux 1 High Warning Enable	1: Enable.	1
			5	Mod Aux 1 Low Warning Enable	1: Enable.	1
			4	Mod Aux 1 Low Alarm Enable	1: Enable.	1
			3	Mod Aux 2 High Alarm Enable	1: Enable.	1
			2	Mod Aux 2 High Warning Enable	1: Enable.	1
			1	Mod Aux 2 Low Warning Enable	1: Enable.	1
			0	Mod Aux 2 Low Alarm Enable	1: Enable.	1
A02D [2.2]	**11**	**RW**		**Vendor Specific FAWS Enable**	**(Optional) Vendor Specified Module Fault, Alarm, Warning and Status Enable. Contents are specified by the vendor.**	**0000h**
A02E	**1**	**RO**		**Reserved**		**0000h**
Module Analog A/D Value Registers						
A02F	**1**	**RO**	**15~0**	**Module Temp Monitor A/D Value**	**Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius,**	**0000h**

CFP Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
					representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C. Accuracy shall be better than +/- 3 degC over the whole temperature range.	
A030	**1**	**RO**	**15~0**	**Module Power supply 3.3 V Monitor A/D Value**	**Internally measured transceiver supply voltage, a 16-bit unsigned integer with LSB = 0.1 mV, yielding a total measurement range of 0 to 6.5535 Volts. Accuracy shall be better than +/-3% of the nominal value over specified operating temperature and voltage range.**	**0000h**
A031	**1**	**RO**	**15~0**	**SOA Bias Current A/D Value**	**Measured SOA bias current in uA, a 16-bit unsigned integer with LSB = 2 uA, representing a total range of from 0 to 131.072 mA. Accuracy shall be better than +/-10% of the nominal value over specified temperature and voltage.**	**0000h**
A032	**1**	**RO**	**15~0**	**Module Auxiliary 1 Monitor A/D Value**	**Definition depending upon the designated use.**	**0000h**
A033	**1**	**RO**	**15~0**	**Module Auxiliary 2 Monitor A/D Value**	**Definition depending upon the designated use.**	**0000h**
A034	**4**	**RO**		**Reserved**		
Module PRBS Registers						
A038	**1**	**RO**		**Network Lane PRBS Data Bit Count**	**Network lane data bit counter increments when network lane RX PRBS Checker is enabled. It stops counting when RX PRBS Checker is disabled. It uses an ad-hoc format floating point number with 6-bit unsigned exponent and 10-bit unsigned mantissa.**	**0000h**
			15~10	Exponent	6-bit unsigned exponent.	0
			9~0	Mantissa	10-bit mantissa giving better than 0.1% accuracy in bit counts.	0
A039	**1**			**Host Lane PRBS Data Bit Count**	**Host lane data bit counter increments when host side TX PRBS Checker is enabled. It stops counting when TX PRBS Checker is disabled. It uses an ad-hoc format floating point number with 6-bit unsigned exponent and 10-bit unsigned mantissa.**	**0000h**
		RO	15~10	Exponent	6-bit unsigned exponent	0
		RO	9~0	Mantissa	10-bit mantissa giving better than 0.1% accuracy in bit counts.	0
A03A	**2**	**RO**		**Reserved**		**0**
Host Configured Receive Optical Power Threshold Values						
A03C [2.2]	**1**	**RW**	**15~0**	**Host Configured Receive Optical Power High Alarm Threshold**	**Valid if the value is between "Host Configured Receive Optical Power High Alarm Permissible Minimum Threshold" (80E8h) and "Host Configured Receive Optical Power High Alarm Permissible Maximum Threshold" (80F0h). Value beyond the threshold shall generate no effect.**	**0**
A03D [2.2]	**1**	**RW**	**15~0**	**Host Configured Receive Optical Power High Warning Threshold**	**Valid if the value is between "Host Configured Optical Power High Warning Permissible Minimum Threshold" (0x80EA) and "Host Configured Optical Power High Warning Permissible Maximum Threshold" (80F2h). Value beyond the threshold shall generate no effect.**	**0**
A03E [2.2]	**1**	**RW**	**15~0**	**Host Configured Receive Optical Power Low Warning Threshold**	**Valid if the value is between "Host Configured Optical Power Low Warning Permissible Minimum Threshold" (80ECh) and "Host Configured Optical Power Low Warning Permissible Maximum Threshold" (80F4h). Value beyond the threshold shall generate no effect.**	**0**
A03F [2.2]	**1**	**RW**	**15~0**	**Host Configured Receive Optical Power Low Alarm Threshold**	**Valid if the value is between "Host Configured Receive Optical Power Low Alarm Permissible Minimum Threshold" (80EEh) and "Host Configured Receive Optical Power Low Alarm Permissible Maximum Threshold" (80F6h). Value beyond the threshold shall generate no effect.**	**0**
A040	**64**	**RO**		**Reserved**		**0**

5.6 MLG Management Interface Register Table

Table 28 MLG VR 1 contains registers to configure and monitor Multi-Link Gearbox features on the module if this feature is supported. (This is a preliminary proposal. If any vendor or user desires to implement it please contact CFP MSA MIS Editor).

Table 28 MLG VR 1

MLG VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
MLG Management Interface						
A080 [2.2]	**1**	**RW**		**Generic MLG Management**		**0000h**
			15	MLG MUX Enable	0: disable mux, 1: enable mux	0
			14	MLG DEMUX Enable	0: disable demux, 1: enable demux	0
			13~10	Reserved		0000b
			9~0	Lane n Loopback Enable	Lane number n ranges from 9 to 0. 0: disable loopback, 1: enable loopback	0
A081 [2.2]	**1**	**RW**		**MLG MUX 10G Lane Enable**		**0000h**
			15~10	Reserved		00h
			9~0	Lane n Enable	Lane number n ranges from 9 to 0. 0: disable lane, 1: enable lane	0
A082 [2.2]	**1**	**RW**		**MLG MUX 10G Output Timing Reference**		**0000h**
			15~4	Reserved		000h
			3~0	10G Timing Reference Lane Index	0000b: lane 0, 1001b: lane 9, All other codes undefined.	0000b
A083 [2.2]	**1**	**RW**		**MLG MUX Scrambled Idle Enable**	**Enables or disables the scrambled idle test pattern generated on a given 10G lane**	**0000**
			15~10	Reserved		0
			9~0	Lane n Enable	Lane number n ranges from 9 to 0. 0: disable lane, 1: enable lane	0
A084 [2.2]	**4**	**RO**		**Reserved**	**Reserved**	**0000h**
A088 [2.2]	**1**	**RO**		**MLG MUX Status**	**MLG MUX status variable**	**0000h**
			15	Scrambled Idle Ability	Indicates whether this implementation of MLG has the ability to generate the 10G scrambled idle test pattern on each 10G lane. 0: has no ability, 1: has the ability	0
			14~10	Reserved		00h
			9~0	Lane n Detected	Indicates whether a 10GBASE-R signal was successfully recovered through CDR and the 66B block lock process on each of the input lanes. Lane number n ranges from 9 to 0. 0: not detected 1: detected.	0
A089 [2.2]	**7**	**RO**		**Reserved**	**Reserved**	**0000h**
A090 [2.2]	**1**	**RW**		**MLG DEMUX 10G Lane Enable**	**Enables or disables each of the 10G output lanes.**	**0000h**
			15~10	Reserved		00h
			9~0	Lane n Enable	Bit 9 corresponding to Lane 9. Bit 0 corresponding to Lane 0. 0: disable; 1: enable	0
A091 [2.2]	**1**	**RW**		**MLG DEMUX Scrambled Idle Enable**	**if implemented, enables or disables the scrambled idle test pattern checker for the indicated 10G lane.**	**0000h**
			15~10	Reserved		00h
			9~0	Lane n Enable	Bit 9 corresponding to Lane 9. Bit 0 corresponding to Lane 0. 0: disable; 1: enable	0
A092 [2.2]	**6**	**RO**		**Reserved**	**Reserved**	**0000h**

MLG VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
A098 [2.2]	**1**	**RO**		**MLG DEMUX Status**	**Indicates whether the input lanes of the MLG demux are being received at the PMA(n:20). Depending on n, individual lane status variables may be available. Since n is implementation dependent, so are the status registers.**	**0000h**
			15	Scrambled Idle Ability	Indicates whether this implementation of MLG has the ability to generate the 10G scrambled idle test pattern on each 10G lane. 0: has no ability, 1: has the ability	0
			14~4	Reserved		000h
			3~0	Lane n Received	Indicates whether the input lanes of the MLG demux are being received at the PMA(n:20). Depending on n, individual lane status variables may be available. Since n is implementation dependent, so are the status registers. 0: not received, 1: received	0
A099 [2.2]	**1**	**RO**		**MLG DEMUX Block Lock 1**	**Indicate whether 66B block lock has been achieved on each of the MLG lanes**	**0000h**
			15~4	Reserved		000h
			3~0	MLG Lane n Achieved	Bit 3 maps to Lane 19, Bit 2 maps to Lane 18, Bit 1 maps to Lane 17, Bit 0 maps to Lane 16. 0: Not Achieved, 1: Achieved	0
A09A [2.2]	**1**	**RO**		**MLG DEMUX Block Lock 0**	**Indicate whether 66B block lock has been achieved on each of the MLG lanes**	**0000h**
			15~0	MLG Lane n Achieved	Bit n maps to Lane n, respectively. n ranges from 15 to 0. 0: Not Achieved, 1: Achieved	0
A09B [2.2]	**1**	**RO**		**MLG DEMUX AM Lock 1**	**Indicates whether alignment marker lock has been achieved on each of the MLG lanes**	**0000h**
			15~4	Reserved		000h
			3	MLG Lane 19 Achieved	0: Not Achieved, 1: Achieved	0
			2	MLG Lane 18 Achieved	0: Not Achieved, 1: Achieved	0
			1	MLG Lane 17 Achieved	0: Not Achieved, 1: Achieved	0
			0	MLG Lane 16 Achieved	0: Not Achieved, 1: Achieved	0
A09C [2.2]	**1**	**RO**		**MLG DEMUX AM Lock 0**	**Indicates whether alignment marker lock has been achieved on each of the MLG lanes**	**0000h**
			15~0	MLG Lane n Achieved	Bit n maps to Lane n respectively. 0: Not Achieved, 1: Achieved	0
A09D [2.2]	**1**	**RO**		**MLG DEMUX Lane Alignment Status 1**	**Indicates whether all 20 lanes have achieved lane alignment marker lock, that the 20 distinct lane markers are received, and inter-MLG lane skew permits the 10GBASE-R signals to be reassembled.**	**0000h**
			15~4	Reserved		000h
			3	MLG Lane 19 Achieved	0: Not Achieved, 1: Achieved	0
			2	MLG Lane 18 Achieved	0: Not Achieved, 1: Achieved	0
			1	MLG Lane 17 Achieved	0: Not Achieved, 1: Achieved	0
			0	MLG Lane 16 Achieved	0: Not Achieved, 1: Achieved	0
A09E [2.2]	**1**	**RO**		**MLG DEMUX Lane Alignment Status 0**	**Indicates whether all 20 lanes have achieved lane alignment marker lock, that the 20 distinct lane markers are received, and inter-MLG lane skew permits the 10GBASE-R signals to be reassembled.**	**0000h**
			15~0	MLG Lane n Achieved	Bit n maps to Lane n respectively. 0: Not Achieved, 1: Achieved	0
A09F [2.2]	**1**	**RO**		**Reserved**	**Reserved**	**0000h**
A0A0 [2.2]	**20**	**RO**		**MLG DEMUX BIP Error Counter MLG Lane n**	**Contains the count of BIP errors counted on each MLG lane.** **It uses an ad-hoc format floating point number with 6-bit unsigned exponent and 10-bit unsigned mantissa, same format as register A039.** **Register A0A0h maps to Lane 19, …, Register A0B3h maps to Lane 0.**	**0000h**

MLG VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
A0B4 [2.2]	**12**	**RO**		**Reserved**		**0000h**
A0C0 [2.2]	**20**	**RO**		**MLG DEMUX Logic Lane Mapping on Position n**	**Indicates which (logical) MLG lane is received in each MLG lane position. Note that the MLG lanes that may be received in a MLG lane position are numbered 0.0, 0.1, 1.0, …, 9.1. Format: 0x00xy represents logic lane number (x.y). Register A0C0h maps to Lane 19, …, Register A0D3h maps to Lane 0.**	**0000h**
A0D4 [2.2]	**12**	**RO**		**Reserved**		**0000h**
A0E0 [2.2]	**10**	**RO**		**MLG DEMUX Scrambled Idle Error Lane n**	Register A0E0h contains value of Lane 9. … Register A0E9h contains value of Lane 0.	**0000h**
A0EA	**22**	**RO**		**Reserved**		**0000h**

5.7 Network Lane Specific Register Tables

Table 29 Network Lane VR 1 and *Table 30 Network Lane VR 2* contain network lane specific registers. Each register listed is the nth element of a 16-register array, representing the nth network lane of N total network lanes. The maximum N CFP MSA specifies is 16. All the register information is detailed in the description column. The registers of all the unused lanes shall be set to zero initial value.

In CFP MSA MIS Version 2.2, *Table 31 Network Lane VR 3 (Optional)* is added to support optional Vendor Specific Network Lane FAWS.

Table 29 Network Lane VR 1

Network Lane VR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
Network Lane FAWS Registers						
A200	**16**	**RO**		**Network Lane n Alarm and Warning**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
			15	Bias High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			14	Bias High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			13	Bias Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			12	Bias Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			11	TX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			10	TX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			9	TX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			8	TX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			7	Laser Temperature High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			6	Laser Temperature High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			5	Laser Temperature Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			4	Laser Temperature Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			3	RX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			2	RX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			1	RX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			0	RX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
A210	**16**	**RO**		**Network Lane n Fault and Status**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …,**	**0000h**

Network Lane VR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
					N-1. N_max = 16. Actual N is module dependent.	
			15	Lane TEC Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			14	Lane Wavelength Unlocked Fault	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			13	Lane APD Power Supply Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			12~8	Reserved		0
			7	Lane TX_LOSF	0: Normal; 1: Asserted. (PMD) (FAWS_TYPE_C)	0
			6	Lane TX_LOL	0: Normal; 1: Asserted. (Network) (FAWS_TYPE_B)	0
			5	Reserved		0
			4	Lane RX_LOS	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			3	Lane RX_LOL	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			2	Lane RX FIFO error	0: Normal, 1: Error. (FAWS_TYPE_B)	0
			1	Reserved.		0
			0	Reserved.		0
Network Lane FAWS Latch Registers						
A220	**16**	**RO/LH/COR**		**Network Lane n Alarm and Warning Latch**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
			15	Bias High Alarm Latch	1: Latched.	0
			14	Bias High Warning Latch	1: Latched.	0
			13	Bias Low Warning Latch	1: Latched.	0
			12	Bias Low Alarm Latch	1: Latched.	0
			11	TX Power High Alarm Latch	1: Latched.	0
			10	TX Power High Warning Latch	1: Latched.	0
			9	TX Power Low Warning Latch	1: Latched.	0
			8	TX Power Low Alarm Latch	1: Latched.	0
			7	Laser Temperature High Alarm Latch	1: Latched.	0
			6	Laser Temperature High Warning Latch	1: Latched.	0
			5	Laser Temperature Low Warning Latch	1: Latched.	0
			4	Laser Temperature Low Alarm Latch	1: Latched.	0
			3	RX Power High Alarm Latch	1: Latched.	0
			2	RX Power High Warning Latch	1: Latched.	0
			1	RX Power Low Warning Latch	1: Latched.	0
			0	RX Power Low Alarm Latch	1: Latched.	0
A230	**16**			**Network Lane n Fault and Status Latch**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
		RO/LH/COR	15	Lane TEC Fault Latch	1: Latched.	0
		RO/LH/COR	14	Lane Wavelength Unlocked Fault Latch	1: Latched.	0
		RO/LH/COR	13	Lane APD Power Supply Fault Latch	1: Latched.	0
		RO	12~8	Reserved		0
		RO/LH/COR	7	Lane TX_LOSF Latch	1: Latched.	0
		RO/LH/COR	6	Lane TX_LOL Latch	1: Latched.	0
		RO	5	Reserved		0

Network Lane VR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
		RO/LH/COR	4	Lane RX_LOS Latch	1: Latched.	0
		RO/LH/COR	3	Lane RX_LOL Latch	1: Latched.	0
		RO/LH/COR	2	Lane RX FIFO Status Latch	1: Latched.	0
		RO	1~0	Reserved		0
Network Lane FAWS Enable Registers						
A240	**16**	**RW**		**Network Lane n Alarm and Warning Enable**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**FFFFh**
			15	Bias High Alarm Enable	0: Disable, 1: Enable.	1
			14	Bias High Warning Enable	0: Disable, 1: Enable.	1
			13	Bias Low Warning Enable	0: Disable, 1: Enable.	1
			12	Bias Low Alarm Enable	0: Disable, 1: Enable.	1
			11	TX Power High Alarm Enable	0: Disable, 1: Enable.	1
			10	TX Power High Warning Enable	0: Disable, 1: Enable.	1
			9	TX Power Low Warning Enable	0: Disable, 1: Enable.	1
			8	TX Power Low Alarm Enable	0: Disable, 1: Enable.	1
			7	Laser Temperature High Alarm Enable	0: Disable, 1: Enable.	1
			6	Laser Temperature High Warning Enable	0: Disable, 1: Enable.	1
			5	Laser Temperature Low Warning Enable	0: Disable, 1: Enable.	1
			4	Laser Temperature Low Alarm Enable	0: Disable, 1: Enable.	1
			3	RX Power High Alarm Enable	0: Disable, 1: Enable.	1
			2	RX Power High Warning Enable	0: Disable, 1: Enable.	1
			1	RX Power Low Warning Enable	0: Disable, 1: Enable.	1
			0	RX Power Low Alarm Enable	0: Disable, 1: Enable.	1
A250	**16**			**Network Lane n Fault and Status Enable**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**E0DCh**
		RW	15	Lane TEC Fault Enable	0: Disable, 1: Enable.	1
		RW	14	Lane Wavelength Unlocked Fault Enable	0: Disable, 1: Enable.	1
		RW	13	Lane APD Power Supply Fault Enable	0: Disable, 1: Enable.	1
		RO	12~8	Reserved		0
		RW	7	Lane TX_LOSF Enable	0: Disable, 1: Enable.	1
		RW	6	Lane TX_LOL Enable	0: Disable, 1: Enable.	1
		RO	5	Reserved		0
		RW	4	Lane RX_LOS Enable	0: Disable, 1: Enable.	1
		RW	3	Lane RX_LOL Enable	0: Disable, 1: Enable.	1
		RW	2	Lane RX FIFO Status Enable	0: Disable, 1: Enable.	1
		RO	1~0	Reserved		0
A260	**32**	**RO**		**Reserved**		**0000h**

1 *Table 30 Network Lane VR 2*

Network Lane VR 2						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***

Network Lane VR 2						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
Network Lane Control Registers						
A280	**16**			**Network Lane n FEC Controls**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
		RW	15~8	Phase Adjustment	This signed 8-bit value represents the phase set point of receive path quantization relative to 0.5 UI, given by: 0.5UI + (Phase Adjustment) / 256 UI. (Optional function) Set this value = -128 (80h) to de-activate this function.	00h
		RW	7~0	Amplitude Adjustment	This signed 8-bit value represents the amplitude threshold of relative amplitude of receive path quantization relative to 50% (Optional function), given by: 50% + (Amplitude Adjustment) / 256 * 100%. (Optional function) Set this value = -128 (80h) to de-activate this function.	00h
A290	**16**	**RO**	**15~0**	**Network Lane n PRBS Rx Error Count**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** **This counter increases upon detection of each network lane RX checker error when RX PRBS Checker is enabled. It uses an ad-hoc floating point number format with a 6-bit unsigned exponent and a 10-bit unsigned mantissa. Base of exponent is 2 and Mantissa radix is 0.**	**0000h**
			15~10	Exponent	6-bit unsigned exponent.	0
			9~0	Mantissa	10-bit mantissa giving better than 0.1% accuracy in bit counts.	0
Network Lane A/D value Measurement Registers						
A2A0	**16**	**RO**	**15~0**	**Network Lane n Laser Bias Current monitor A/D value**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** **Measured laser bias current in uA, a 16-bit unsigned integer with LSB = 2 uA, representing a total measurement range of 0 to 131.072 mA. Minimum accuracy shall be +/- 10% of the nominal value over temperature and voltage.**	**0000h**
A2B0	**16**	**RO**	**15~0**	**Network Lane n Laser Output Power monitor A/D value**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** **Measured TX output power in uW, a 16-bit unsigned integer with LSB = 0.1 uW, representing a range of laser output power from 0 to 6.5535 mW (-40 to +8.2 dBm). Accuracy must be better than +/- 2 dB over temperature and voltage range. Relative accuracy must be better than 1 dB.**	**0000h**

Network Lane VR 2						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
A2C0	**16**	**RO**	**15~0**	**Network Lane n Laser Temp Monitor A/D value**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C. Minimum accuracy is +/- 3 degC over temperature range.**	**0000h**
A2D0	**16**	**RO**	**15~0**	**Network Lane n Receiver Input Power monitor A/D value**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured received input power in uW, a 16-bit unsigned integer with LSB = 0.1 uW, representing a power range from 0 to 6.5535 mW (-40 to +8.2 dBm). Value can represent either average received power or OMA depending upon how bit 3 of Register 8080h is set. Accuracy must be better than +/- 2dB over temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss per the appropriate standard. Relative accuracy shall be better than 1 dB over the received power range, temperature range, voltage range, and the life of the product.**	**0000h**
A2E0	**32**	**RO**	**15~0**	**Reserved**		**0000h**

Table 31 Network Lane VR 3 (Optional)

Network Lane VR 3						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
Network Lane n Vendor Specific FAWS Registers						
A300 [2.2]	**16**	**RO**	**15~0**	**Network Lane n Vendor Specific FAWS**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. For every bit in each register, 0: Normal; 1: Asserted.**	**0000h**
A310 [2.2]	**16**	**RO/LH/ COR**	**15~0**	**Network Lane n Vendor Specific FAWS Latch**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. For every bit in each register, 0: Normal; 1: Asserted.**	**0000h**
A320 [2.2]	**16**	**RW**	**15~0**	**Network Lane n Vendor Specific FAWS Enable**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. For every bit in each register, 0: Disable; 1: Enable.**	**0000h**
A330	**16**	**RO**	**15~0**	**Reserved**		**0000h**
A340 [2.2]	**16**	**RO**	**15~0**	**Network Lane n Vendor Specific Auxiliary 1 Monitor A/D Value**	**Definition provided by vendor. FAWS mapped to Network Lane n Vendor Specific FAWS bit 15.**	**0000h**
A350 [2.2]	**16**	**RO**	**15~0**	**Network Lane n Vendor Specific Auxiliary 2 Monitor A/D Value**	**Definition provided by vendor. FAWS mapped to Network Lane n Vendor Specific FAWS bit 14.**	**0000h**
A360	**16**	**RO**	**15~0**	**Network Lane n Vendor Specific**	**Definition provided by vendor. FAWS mapped to**	**0000h**

Network Lane VR 3						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
[2.2]				**Auxiliary 3 Monitor A/D Value**	**Network Lane n Vendor Specific FAWS bit 13.**	
A370 [2.2]	**16**	**RO**	**15~0**	**Network Lane n Vendor Specific Auxiliary 4 Monitor A/D Value**	**Definition provided by vendor. FAWS mapped to Network Lane n Vendor Specific FAWS bit 12.**	**0000h**

5.8 Host lane Specific Register Table

Table 32 Host Lane VR 1 contains host lane specific registers. Each register listed is the m^th^ element of a 16-register array, representing the m^th^ host lane of M total host lanes. The maximum M CFP MSA specifies is 16. All the register information is detailed in the description column. The registers of all the unused lanes shall be set to zero initial value.

Table 32 Host Lane VR 1

Host Lane VR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
Host Lane FAWS Status Registers						
A400	**16**			**Host Lane m Fault and Status**	**16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …, M-1. M_max = 16. Actual M is module dependent.**	**0000h**
		RO	15~2	Reserved		0
		RO	1	Lane TX FIFO Error	Lane specific TX FIFO error. (FAWS_TYPE_B) 0: Normal, 1: Error.	0
		RO	0	TX_HOST_LOL	TX IC Lock Indicator, (FAWS_TYPE_B) 0: Locked, 1: Loss of lock.	0
Host Lane FAWS Latch Registers						
A410	**16**			**Host Lane m Fault and Status Latch**	**16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …, M-1. M_max = 16. Actual M is module dependent.**	**0000h**
		RO	15~2	Reserved		0
		RO/LH/COR	1	Lane TX FIFO Error Latch	1: Latched.	0
		RO/LH/COR	0	TX_HOST_LOL Latch	1: Latched.	0
Host Lane FAWS Enable Registers						
A420	**16**			**Host Lane m Fault and Status Enable**	**16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …, M-1. M_max = 16. Actual M is module dependent.**	**0001h**
		RO	15~2	Reserved		0
		RW	1	Lane TX FIFO Error Enable	1: Enable.	0
		RW	0	TX_HOST_LOL Enable	1: Enable.	1
Host Lane Digital PRBS Registers						
A430	**16**	**RO**		**Host Lane m PRBS TX Error Count**	**16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …, M-1. M_max = 16. Actual M is module dependent. This counter increases upon detection of each RX checker error when host lane TX PRBS checker is enabled. It stops counting when the TX PRBS checker is disabled. It uses an ad-hoc floating point number format with a 6-bit unsigned exponent and a 10-bit unsigned mantissa.**	**0000h**
			15~10	Exponent	6-bit unsigned exponent.	0

Host Lane VR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
			9~0	Mantissa	10-bit mantissa giving better than 0.1% accuracy in bit counts.	0
Host Lane Control Registers						
A440	**16**			**Host Lane m Control**	**16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …, M-1. M_max = 16. Actual M is module dependent.**	**0007h**
		RW	15	Signal equalization mode control	0: Automatic, 1: Manual.	0
		RW	14~8	Signal Equalization	A 7-bit unsigned integer: 0~63: Reserved values by MSA, 64~127: Vendor specific values	0
		RO	7~4	Reserved		0
		RW	3~0	Signal Pre/De-emphasis	4-bit unsigned number N represents the pre/de-emphasis applied. Pre/De-emphasis = N * 0.5 dB, N = 0, …, 15. The power on default is 3.5 dB with a value of 7 in this field.	7
A450	**48**	**RO**		**Reserved**		**0000h**

6 MSA-100GLH MODULE MANAGEMENT INTERFACE

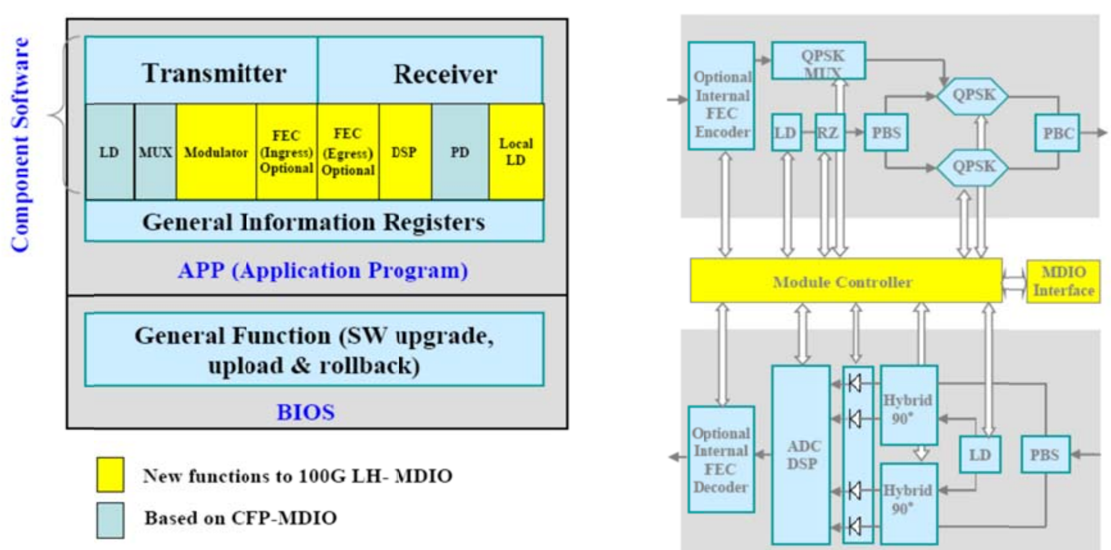
6.1 Overview

This section specifies an extension to the CFP MSA Management Interface Specification for supporting the OIF 100G Long-Haul DWDM Transmission Module Electro-mechanical MSA (MSA-100GLH) (Reference 6). The MSA-100GLH specifies the use of MDIO [2] as the management interface between a Host and MSA-100GLH Module. The intention of including the MSA-100GLH management interface specification in the CFP MSA MIS document is to enable a common host-module management interface implementation that encompasses both 100Gb/s client and line-side optical transmission module applications.

MDIO registers and functionality required for supporting the MSA-100GLH application are specified in this section. Optical transport networking and modulation format dependent register options are also specified. This specification strives to remain modulation format and data rate agnostic whenever practical to maximize applicability to future market requirements.

The MSA-100GLH module management software architecture and logical relationship to the MSA-100GLH module hardware architecture are illustrated in
. The MSA-100GLH module software and hardware architectures depicted in this Figure are for illustration purposes only and do not imply implementation requirements. When multiple MSA-100GLH modules are connected via a single bus, a particular MSA-100GLH module may be selected by using the MDIO Physical Port Address pins.

Figure 15 MSA-100GLH Module Management Architecture



6.2 MSA-100GLH Module Management Interface Information & Functionality

The following management information and functionality are specified for the MSA-100GLH Management Interface in addition to the management information and functionality specified in the Sections 4 and 5 of this document. The additional information and functionality specified in this section are categorized as follows:

1. Module Base and Extended ID Information
2. Module Level Commands, Control & FAWS
3. MDIO Write Flow Control
4. Module Additional Monitored Parameters
5. Performance Monitoring (including optional FEC, OTN and modulation format dependent optical parameters)
6. Software Upgrade Capability
7. Auxiliary Channel over MDIO (Optional)
8. Module-to-Host Generic Data Upload Capability
9. Bulk Data Transfer Procedure

6.2.1 Module Base and Extended ID Information

Base and extended information registers specified in Section 5 are modified to support the MSA-100GLH application from CFP MSA MIS Version 2.2.

6.2.2 Module Command, Control & FAWS

Module level command setup, control and status registers defined in Sections 4 and 5 are modified and extended to support the MSA-100GLH application. Additional control parameters necessary for the MSA-100GLH application include:

- Password Control (Option);
- TX laser frequency and power control;
- RX laser frequency control;
- FEC control;
- Host lane signal equalization control.

These major additions stem from the MSA-100GLH module having a tunable frequency for DWDM operation and having an additional laser for the Network Receive interface for coherent operation.

6.2.2.1 Password Control (Optional)

Password control is optionally provided in this MSA to allow vendor and user control of access to information in the register shadow. Registers B000h ~ B001h are reserved for the password entry. If this option is not supported, these registers shall be read as 00000000h. Otherwise, these registers shall be read as FFFFFFFFh. Register access under password control is shown in *Table 33 Register Access Password Requirements*. If this option is not supported, any entries in the table that are not marked as N/A do not require a password.

When password control is supported, the password entry registers are write-only (WO) and shall always read FFFFFFFFh. Any values written to these registers are retained until Reset or rewritten by the host. Password is a 2-word long data with the most significant word occupying the lower register address. Password values for the user shall be in the range of 00000000h to 7FFFFFFFh. Password values for the vendor shall be in the range of 80000000h to FFFFFFFFh. MSA defines the default user password value as 01011100h. *Table 11: Register Access Password* lists the access control required for MSA defined registers.

6.2.2.1.1 Power On/Reset Password Initialization

On power up and reset, the Password Entry registers shall be initialized to 00000000h. The initialized contents of the Password Entry registers are compared to the previously stored password value. If the previously stored password value is 00000000h, full access to password protected registers shall be allowed. Note that even though the internal contents of these registers have been initialized to 00000000h, a read of these registers by the host shall return FFFFFFFFh.

6.2.2.1.2 Password Entry (need to put same change in as that in Chap 4)

The password shall be entered by writing a value to registers B000h and B001h. If the contents of both registers match to the previously stored password value, full access to password protected registers shall be allowed. If the contents do not match to the previously stored password, any access to password protected registers shall not be allowed.

6.2.2.1.3 Password Change

The user password can be changed by writing the new value to the Password Change registers B002h and B003h after a password entry is successful. The new password value shall be stored and take effect only after writing the Save User Password command to register B004h.

Table 33 Register Access Password Requirements

Register	Read	Write	Restore	Save	Note
Module NVR Tables	Not Required	N/A	N/A	N/A	*Using register A004h to operate
Vendor NVR Tables	Required	N/A	N/A	N/A	
User NVR Tables	Required	Required	Required *	Required *	
Module VR Tables	Not Required	Not Required	N/A	N/A	

6.2.2.2 Laser Frequency Setting Definition

The TX laser frequency as a function of channel number is defined as:

Freq(GHz) = (Tx_chan_no (B400h.9~0) - 1) * Tx_grid_spacing (B400h.15~13) + chan_1_freq (818Ah*1000, 818Ch/20) + Tx_fine_tune_freq (B430h/1000)

The RX laser frequency as a function of channel number is defined as:

Freq(GHz) = (Rx_chan_no (B420h.9~0) - 1) * Rx_grid_spacing (B420h.15~13) + chan_1_freq (818Ah*1000, 818Ch/20) + Rx_fine_tune_freq (B440h/1000)

The fine tune frequency registers B430h(TX) and B440h(Rx) should be set under the low power state to avoid the mis-setting of laser frequency.

Related registers channel number, grid spacing (B400h, B420h) and fine frequency tuning (B430h, B440h) are settable parameters from the host. First channel and last channel frequency (for each system vendor) are defined by the module at registers 818Ah, 818Ch, 818Eh and 818Gh. Registers B450h ~ B480h give current laser frequency settings in the module.

Note: Registers 0x8012h, 0x8014h and 0x8016h provide module transmitter spectral characteristics information for all applications. However, they do not have a role in transmitter wavelength provisioning between host and module.

6.2.2.3 MSA-100GLH Module Global Alarm System Logic

Modifications to the CFP Global Alarm system logic specified in Section 6.2.2.3 for the MSA-100GLH module application is described below.

The MSA-100GLH module uses GLB_ALRM, to alert the Host any condition outside normal operating conditions. The GLB_ALRM is related to all the contributing FAWS registers including the status registers, the latch registers, and the enable registers, all listed in *Table 34 MSA-100GLH Global Alarm Related Registers*.

Figure 16 MSA-100GLH Module Global Alarm Signal Aggregation depicts the global alarm signal aggregation logic. In this system, status registers drive the latch registers on a bit-by-bit basis. The logic OR of all enabled bits in the latched registers drives GLB_ALRM. This simple and flat OR combinational logic minimizes the assert time after a global alarm condition happens.

Also shown in, the Host shall control which latched bits resulting in a global alarm assertion by asserting individual bits in the enable registers. All enabling bits shall be volatile and startup with initial values defined in *Table 27 CFP Module VR 1*.

When GLB_ALRM alerts the Host to a latched condition, the Host may query the latched registers for the condition. The latched bits are cleared on the read of the corresponding register. Thus, a read of all latched registers can be used to clear all latched register bits and to de-assert GLB_ALRM.

Table 34 MSA-100GLH Global Alarm Related Registers

Description	CFP Register Addresses

Summary Registers	
Global Alarm Summary	B018h
Network Lane Alarm and Warning 1 Summary	B019h
Network Lane Fault and Status Summary	B01Ah
Host Lane Fault and Status Summary	B01Bh
Network Lane Alarm and Warning 2 Summary	B01Ch
Status Registers	
Module State	B016h
Module General Status	B01Dh
Module Fault Status	B01Eh
Module Alarm and Warning 1	B01Fh
Module Alarm and Warning 2	B020h
Module Extended Functions	B050h
Network Lane n Alarm and Warning 1	B180h + n, n= 0, 1, …, N-1.
Network Lane n Alarm and Warning 2	B190h + n, n= 0, 1, …, N-1.
Network Lane n Fault and Status	B1A0h + n, n= 0, 1, …, N-1.
Network Lane TX Alignment Status	B210h + n, n= 0, 1, …, N-1.
Network Lane TX Alignment Status PM Interval	B240h + n, n= 0, 1, …, N-1.
Network Lane RX Alignment Status	B250h + n, n= 0, 1, …, N-1.
Network Lane RX Alignment Status PM Interval	B280h + n, n= 0, 1, …, N-1.
Network Lane RX OTN Status	B580h + n, n= 0, 1, …, N-1.
Network Lane RX OTN Status PM Interval	B5B0h + n, n= 0, 1, …, N-1.
Host Lane m Fault and Status	B600h + m, m= 0, 1, …, M-1.
Host Lane TX Alignment Status	B650h + m, m= 0, 1, …, M-1.
Host Lane TX Alignment Status PM Interval	B680h + m, m= 0, 1, …, M-1.
Host Lane RX Alignment Status	B690h + m, m= 0, 1, …, M-1.
Host Lane RX Alignment Status PM Interval	B6C0h + m, m= 0, 1, …, M-1.
Host Lane TX OTN Status	B700h + m, m= 0, 1, …, M-1.
Host Lane TX OTN Status PM Interval	B730h + m, m= 0, 1, …, M-1.
Latch Registers	
Module State Latch	B022h
Module General Status Latch	B023h
Module Fault Status Latch	B024h
Module Alarm and Warning 1 Latch	B025h
Module Alarm and Warning 2 Latch	B026h
Module Extended Functions Latch	B054h
Network Lane n Alarm and Warning 1 Latch	B1B0h + n, n = 0, 1, …, N-1.
Network Lane n Alarm and Warning 2 Latch	B1C0h + n, n = 0, 1, …, N-1.
Network Lane n Fault and Status Latch	B1D0h + n, n = 0, 1, …, N-1.
Network Lane TX Alignment Status Latch	B220h
Network Lane RX Alignment Status Latch	B260h
Network Lane RX OTN Status Latch	B590h + n, n= 0, 1, …, N-1.
Host Lane m Fault and Status Latch	B610h + m, m = 0, 1, …, M-1.
Host Lane TX Alignment Status Latch	B660h
Host Lane RX Alignment Status Latch	B6A0h
Host Lane TX OTN Status Latch	B710h + m, m= 0, 1, …, M-1.
Enable Registers	
Module State Enable	B028h
Module General Status Enable	B029h
Module Fault Status Enable	B02Ah
Module Alarm and Warning 1 Enable	B02Bh
Module Alarm and Warning 2 Enable	B02Ch
Module Extended Functions Enable	B057h
Network Lane n Alarm and Warning 1 Enable	B1E0h + n, n = 0, 1, …, N-1.
Network Lane n Alarm and Warning 2 Enable	B1F0h + n, n = 0, 1, …, N-1.
Network Lane n Fault and Status Enable	B200h + n, n = 0, 1, …, N-1.
Network Lane TX Alignment Status Enable	B230h
Network Lane RX Alignment Status Enable	B270h
Network Lane RX OTN Status Enable	B5A0h + n, n= 0, 1, …, N-1.
Host Lane m Fault and Status Enable	B620h + m, m = 0, 1, …, M-1.
Host Lane TX Alignment Status Enable	B670h

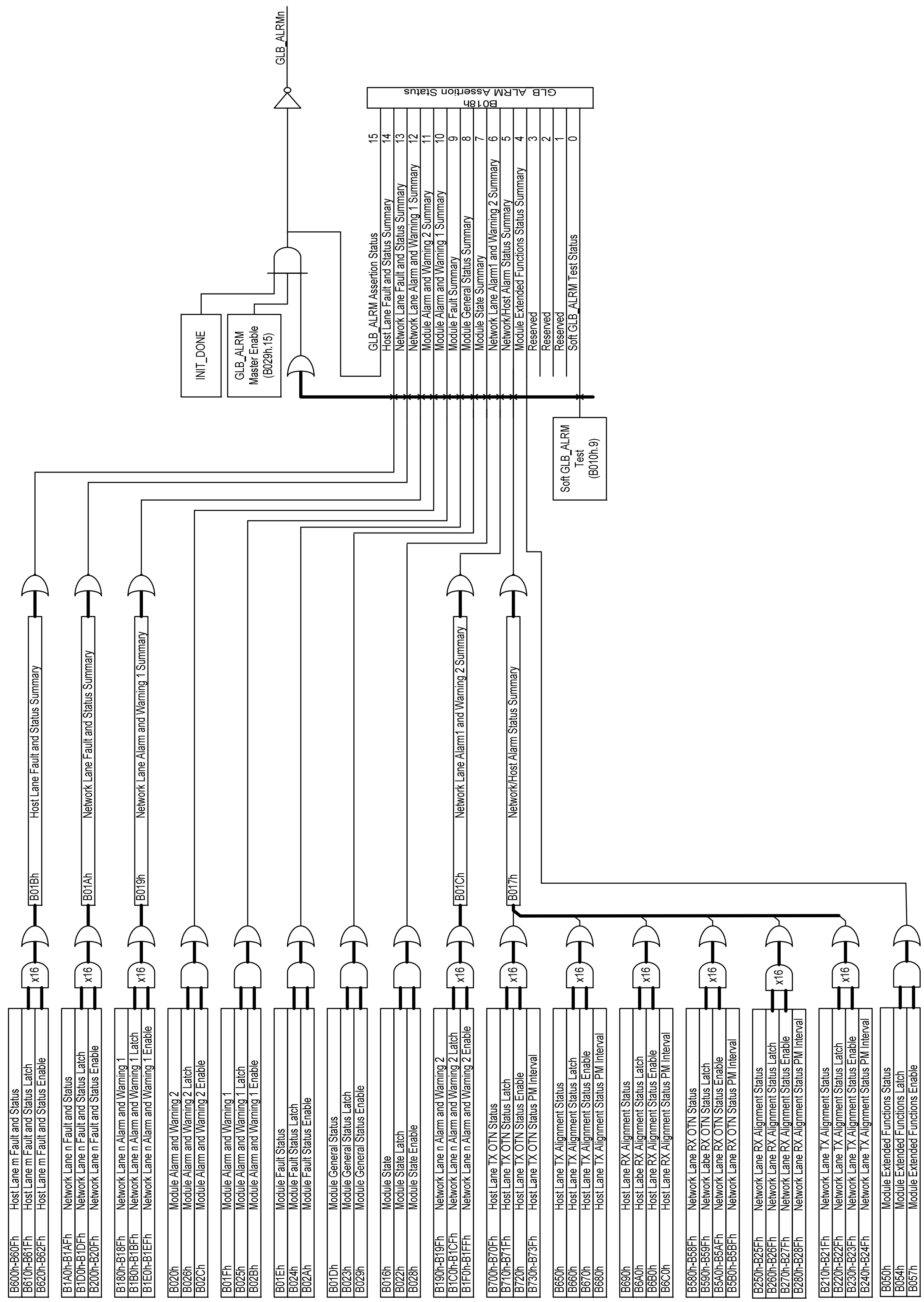
Host Lane RX Alignment Status Enable	B6B0h
Host Lane TX OTN Status Enable	B720h + m, m= 0, 1, …, M-1.
Notes: 1. “n” denotes the network lane index. 2. “N” is the total number of network lanes supported in a MSA-100GLH module. The maximum value of N is 16. 3. “m” denotes the host lane index. 4. “M” is the total number of host lanes supported in a MSA-100GLH module. The maximum value of M is 16.	

In order to minimize the number of reads for locating the origin of the global alarm condition, the Host may use the global alarm query hierarchy listed in *Table 35 Global Alarm Query Hierarchy*.

Table 35 Global Alarm Query Hierarchy

Query Level	CFP Register Name	CFP Register Addresses
1	Global Alarm Summary	B018h
2	Network Lane Alarm and Warning 1 Summary	B019h
2	Network Lane Fault and Status Summary	B01Ah
2	Host Lane Fault and Status Summary	B01Bh
2	Network Lane Alarm and Warning 2 Summary	B01Ch
3	Network Lane n Alarm and Warning 1 Latch	B1B0h + n, n = 0, 1, …, N-1.
3	Network Lane n Alarm and Warning 2 Latch	B1C0h + n, n = 0, 1, …, N-1.
3	Network Lane n Fault and Status Latch	B1D0h + n, n = 0, 1, …, N-1.
3	Host Lane m Fault and Status Latch	B610h + m, m = 0, 1, …, M-1.
Notes: 1. “n” denotes the network lane index. 2. “N” is the total number of network lanes supported in a MSA-100GLH module. The maximum N value is 16. 3. “m” denotes the host lane index. 4. “M” is the total number of host lanes supported in a MSA-100GLH module. The maximum M value is 16.		

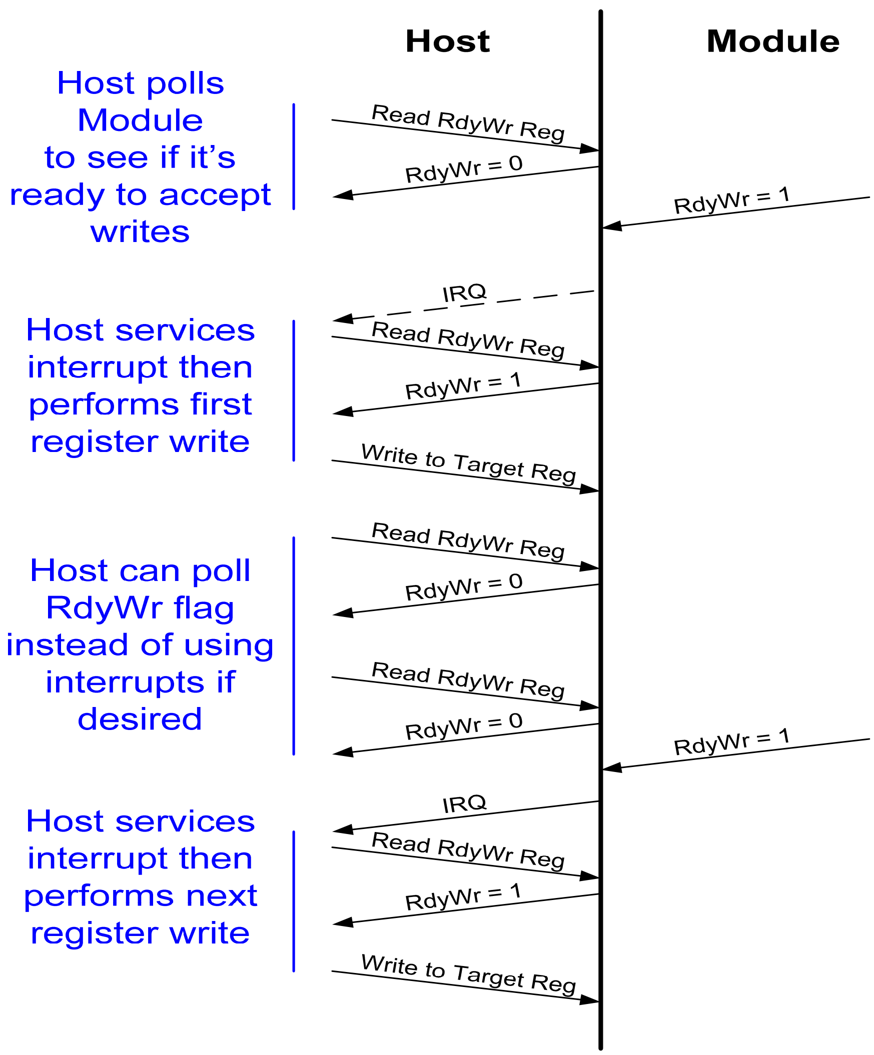
Figure 16 MSA-100GLH Module Global Alarm Signal Aggregation



6.2.3 MDIO Write Flow Control

MDIO Write Flow Control functionality is specified to prevent possible overrun of commands from the host to module that may take relatively longer response time due to software processing, such as setting a laser channel. MDIO Write Flow Control is achieved by defining a status register that has a bit which provides status regarding the completion of the last initiated command and that could also generate an interrupt when command completion occurred. The Host is responsible for querying this register or waiting for a completion interrupt before issuing subsequent MDIO Write transactions. No restrictions are present on MDIO Address, Read or Post Read Increment Address instructions. The Host may execute these commands anytime and as many times per second. The Host and Module interaction for an MDIO Write transaction is illustrated in *Figure 17*.

Figure 17 Host-Module MDIO Write Flow Control



Write Flow Control is applicable only to the 0xB000 page registers defined in Section 6.4. For all registers specified in Section 5, the logic remains the same as in CFP MSA MIS V1.4. If the host is writing to any of the 0xA000 page register, it will just write to the register.

If the host is writing to any of the 0xB000 page register it has to follow the Write Flow Control procedure. Write flow control to 0xBC00-BFFF range bulk data is provided by the registers defined in Module Extended Functions Control Registers.

If the Host writes an MDIO register with an inappropriate value for a field (e.g., power setting not in supported range), the module will set the command error status bit. In addition, the module will provide the MDIO register address at which the error occurred, the data which caused the error, a mask of the specific bits in the data which were in error, and a cause of the error. The host will be informed that an error occurred through the command error status bit, either by polling or as an interrupt. The host can then obtain further details about the error through the supporting Command Error registers. The intent of this facility is to be a diagnostic aid for the host in situations where incorrect data for an MDIO register is written. It is not intended for circumstances where a command is correctly written to an MDIO register, but due to a device error could not be completed successfully, such as if a laser's channel cannot set successfully. Such errors are raised as a fault, alarm or warning as appropriate, via the GLB_ALRMn MDIO interface interrupt mechanism.

6.2.4 Module Monitored Parameters

The following parameters in addition to those specified in the CFP MSA MIS V1.4 are required to be monitored in the MSA-100GLH application:

1. Receiver Laser Bias Current;
2. Receiver Laser Temperature;
3. Receiver Laser Output Power;
4. Transmitter Modulator Bias.

These additional parameters stem from the MSA-100GLH module having an additional Laser for the Network Receive interface for coherent operation and a multi-level/phase modulator for the Network Transmit interface.

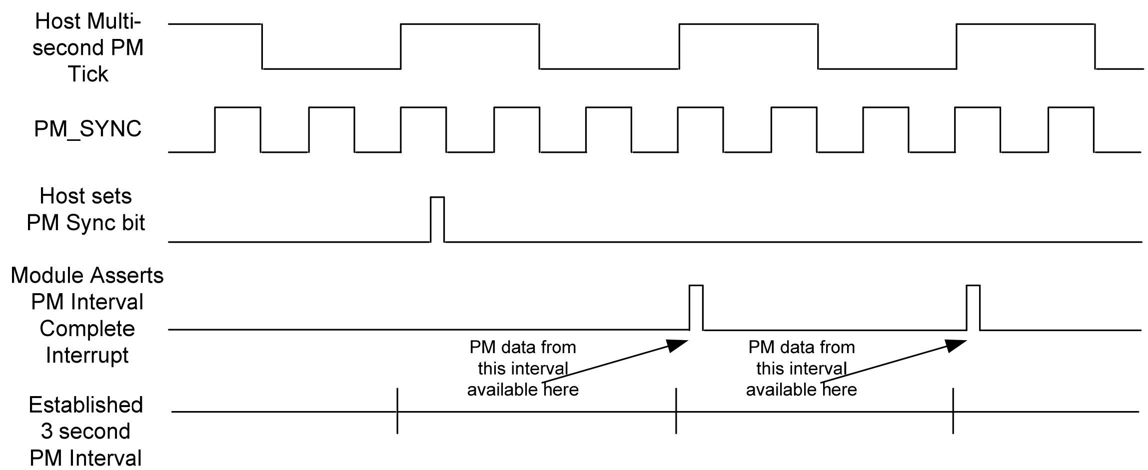
6.2.5 Performance Monitoring

6.2.5.1 Performance Monitoring Tick

The module will have the capability to generate an internal Performance Monitor Tick or use an externally provided one from the host on the PM_SYNC pin. Regardless of the source, the performance monitor tick will have a one second period. The advantage of using the host driven tick is that module Performance Monitoring data can be better synchronized to host data collection, thus avoiding any drift and misalignment between the two. The module will use the one second interval as the basis to provide Performance Monitor data to the host. The host will specify the number of seconds over which it wishes the module to accumulate Performance Monitoring data. This accumulation period can range from 1 second to 64 seconds. At the end of every accumulation period the module can interrupt the host letting it know Performance Monitoring data for a new period is available. The host also has the option to poll for this information. While the last full period data is available to the host, the module is accumulating data for the current period.

The start of a multi-second accumulation period can be specified by the host setting the Performance Monitor Tick Synchronization flag during the one second interval that signifies the start of the multi-second accumulation period. This synchronization may be set any time after module reset. This always indicates beginning of the new period. Any pending period completions will be dropped and the new period starts immediately. For example, if a host has a 3 second PM interval and wishes to synchronize the module to it, then it will first set the Performance Monitor Interval field of the Performance Monitor Control register to 2. Then as shown in *Figure 18* below, it will set the Performance Monitor Tick Synchronization bit and subsequently the module's 3 second PM data will be synchronized with the host.

Figure 18 Host-Module Performance Monitoring Tick Synchronization



In addition to Performance Monitor Tick synchronization with the host, the module can have a one second granularity Real-Time Clock synchronized to the one second performance monitor tick. The Real-Time Clock will specify the time in seconds since Jan. 1, 1970. This will be useful for synchronizing events that occur in the module and could get captured in logs, to events seen on the host.

6.2.5.2 Statistics

The Performance Monitoring statistics that the module provides are described below in *Table 42 MSA-100GLH Network Lane VR 2 Registers*. Modulation format dependent Performance Monitoring statistics are described in Section 6.4.3. Register fields described as "over PM interval" get updated every accumulation period seconds, as specified by the host in the Performance Monitor Interval parameter. The register will have the last value for the previous complete accumulation period. When data for a new accumulation period is available, the module will update the values. FAWS type of parameters will have an "over PM interval" status. This will provide an indication if the FAWS occurred over the last accumulation period. The major parameter additions stem from the MSA-100GLH module being utilized in long distance transmission where optical impairments are significant and the module possibly having a modem in the Network Receive interface for coherent operation.

In addition to having the “over PM interval” status, FAWS type of parameters will also have the module established real-time status, latched status, and interrupt enable functionality.

6.2.5.3 Multi-Word Read Procedure

Some PM Statistics registers are multi-word, e.g. Chromatic Dispersion B800h ~ B810h. There is a possibility that the most and least significant words are inconsistent. For example,

1) Register B800h is read.
2) MW is updated.
3) Register B810h is read.

In this case monitored values are inconsistent.

The follow procedure is specified for MW read:

1) Host sends lower address of MW. -> Module latches appropriate MW data.
2) Host sends Read operation code. -> Module sends Most Significant Word.
3) Host sends upper address of MW.
4) Host sends Read operation code. -> Module sends Least Significant Word.

The example above is then corrected as follows:
Host reads B800h (Current Chromatic Dispersion, Most Significant Word) and B810h (Current Chromatic Dispersion, Least Significant Word).

1) Host sends B800h address. -> Module prepares and latches Current Chromatic Dispersion data (32bit).
2) Host sends Read operation code. -> Module sends Most Significant Word (b31~16).
3) Host sends B810h address.
4) Host sends Read operation code. -> Module sends Least Significant Word (b15~0).

Note: If host sends upper address of MW first, consistency of MW data is not guaranteed.

6.2.6 Software Upgrade Capability

For software upgrade, the software data image must be divided into blocks whose size is determined by how much data can be processed by the module in a given time cycle. Each block includes the data and CRC, so that the module can check whether there are any errors after receiving the block. Upon finding any errors in the block, the module informs the Host of a received errored block and the host must retransmit the same block.

A software upgrade transfer begins with the Host issuing a request to download an image. The module grants the request and the image is written a block at a time in the 0xBC00 address space and setting the “Upgrade Data Block Ready” flag and the module processes each block and updates the status. It is the host responsibility to make sure that each block size is equal to or less than the “Maximum Upgrade Data Block Size”. If there is any error in block processing, the host will retransmit the block. It is recommended to force an abort by the host if a CRC error occurs few times on the same block. While download is not complete, the Host can issue “Abort” command to abort the current download that is in

progress. After all the words of the image have been written to the module, termination of the transfer is completed by issuing a Download Complete to the Upgrade Command register. The module will acknowledge the complete image has been downloaded successfully by providing a Command completed successfully status. If the image had an error in download, then the module will reply with a Command failed status. This state machine is illustrated in
Figure 19 Software Upgrade State Machine. The Software Upgrade sequence is illustrated in. Module sets Maximum Upgrade Data Block Size.

Once the image has been downloaded successfully, the image's service affectability will be reported and a request to run downloaded image can be performed. Ideally, most upgrades should not be service affecting, i.e. services actively supported by the transmission system, especially if they are just software upgrades. In some instances when upgrading firmware it may not be possible to achieve a non-service affecting upgrade. With the image service affecting status provided, the host software can be informed of the side effects that may impact current service by upgrading to the downloaded image. During a service affecting upgrade, the module may be in a state where even MDIO transactions are not available to the module while the upgrade is happening. In order for the host to be cognizant of when MDIO transactions are available, the assertion of the GLB_ALRM pin shall signal to the host that initialization due to the upgrade is complete and the MDIO interface is available. Even though an upgrade is service affecting, it shouldn't require a reconfiguration of the module to get it in the operating state that it was in just prior to the upgrade.

After the run downloaded image request is issued by the Host, the module will be running the downloaded version of software. At this point, the Host can commit the image. If the Host wants to keep both banks the same, then issue "Copy Image" command.

Note: The host should be aware that during module software upgrade, the NVR Checksum may be inconsistent due to mismatch of some register values between host and module, e.g. 0x806Ch, 0x807Bh. These registers should be updated and the host, module NVR Checksums consistent after the module software upgrade is successfully completed.

Also, to clarify expected host behavior following module hardware reset, there are cases that need to be considered:

1. Hardware Reset:
Asserting MOD_RSTn will cause a complete reset of the module. All VR values are lost and must be re-written by the Host.

2. Non-service affecting upgrade
Non-service affecting upgrades are typically software-only upgrades and will not include module reprogramming. If the VR is maintained in the module, the MDIO register space is preserved during the upgrade. The CPU must re-read the VR after the upgrade to return to the state prior to the upgrade. This will include channel numbers, power settings etc

3. Service affecting upgrade

Service affecting upgrades may include reprogramming of the module. During this process, the contents of the VR in the module may be lost and the host must reset the VR to return the module to the configuration state prior to the upgrade.

Figure 19 Software Upgrade State Machine

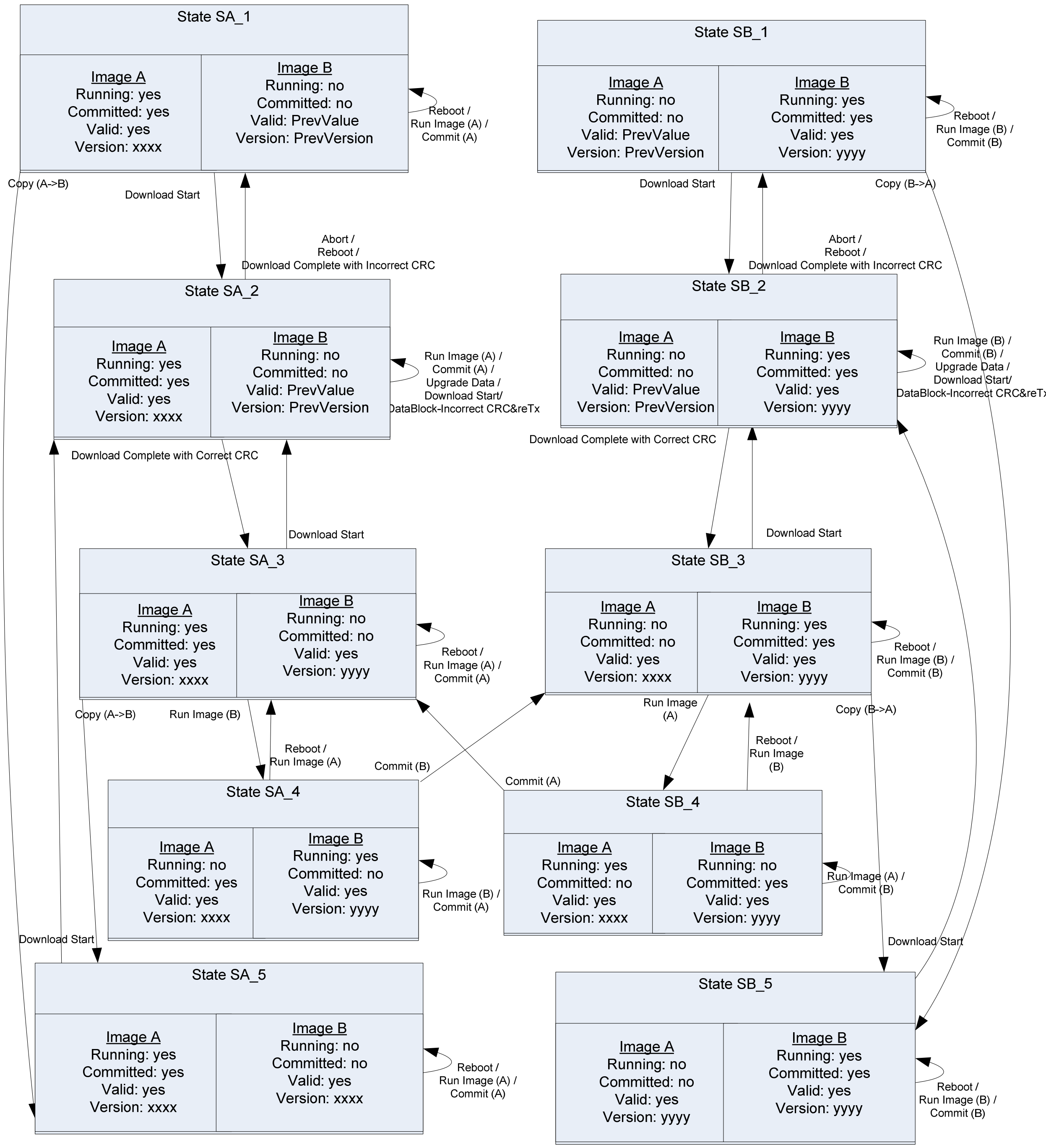
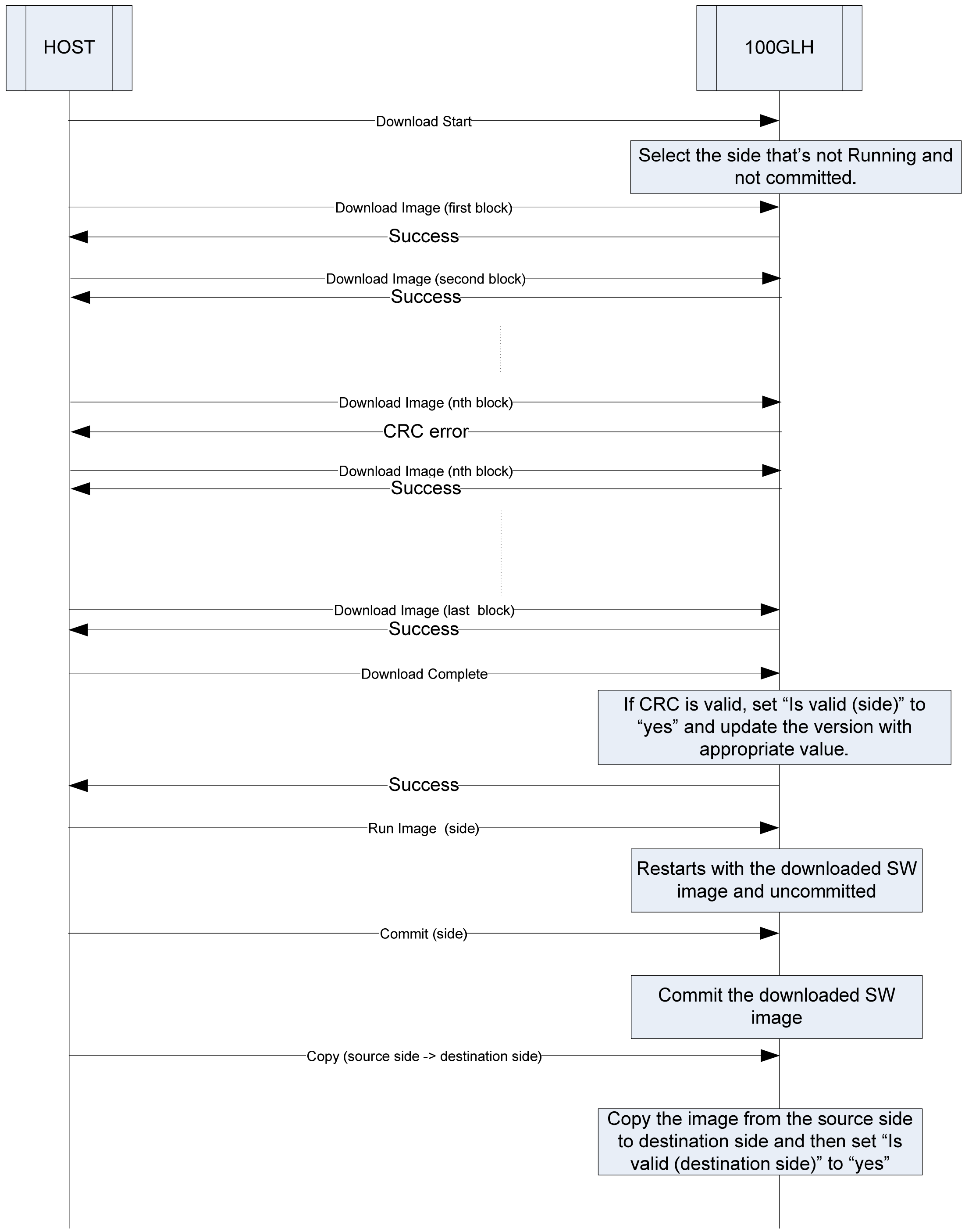


Figure 20 Software Upgrade Sequence

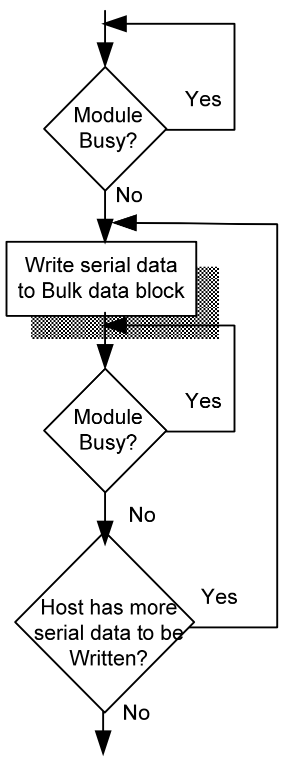


6.2.7 Auxiliary Channel over MDIO (Optional)

Diagnostics and debugging of any module is challenging for many reasons: limited pins, limited register space, lack of accessibility, being embedded in a line-card and shelf that could be of a different manufacturer than the module. In order to alleviate some of these short-comings, a standardized optional Auxiliary interface via MDIO registers is defined. With software support from the line-card and shelf hosting the module, it is envisioned the Auxiliary interface could provide Field Applications Engineers and developers with access to the module for detailed real-time interrogation. One of the usages of this interface is to extend UART support. The UART aspect of the Auxiliary interface means that there is a simple interface, consisting simply of transmit and receive registers without any hardware flow control. Flow control will be inherent via the bulk data transfer MDIO interface. The optional Auxiliary interface will not affect any other MDIO activity, so it should be transparent for normal MDIO status and command execution (with the exception of anything that uses bulk data block).

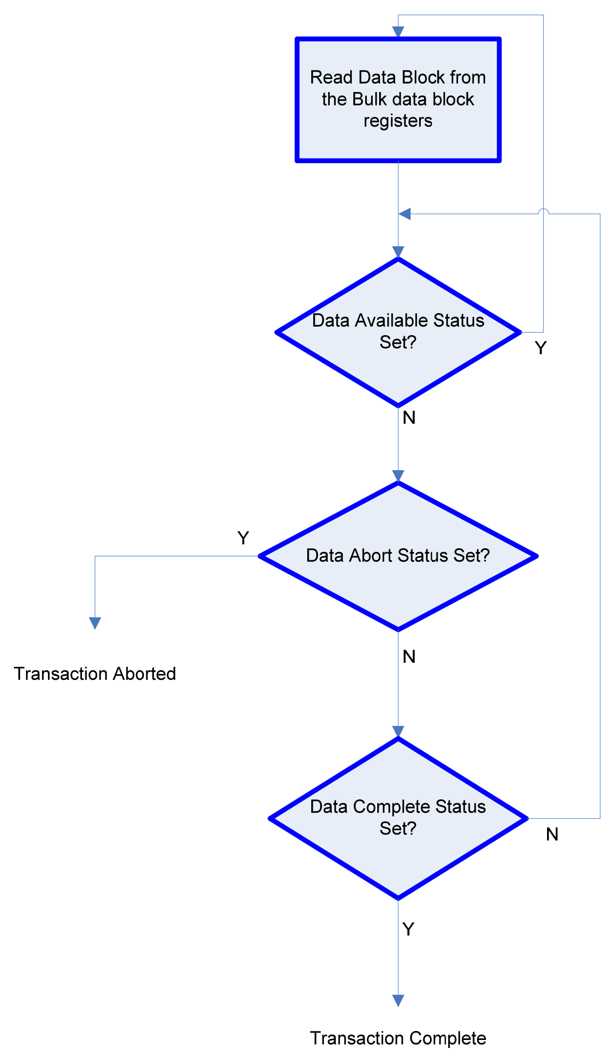
The procedure for host to module data transfer over the Auxiliary interface is shown in *Figure 21 Host-to-Module Auxiliary Interface Data Transfer*. Flow control between the host and module is achieved through the MDIO write flow control mechanism.

Figure 21 Host-to-Module Auxiliary Interface Data Transfer



The procedure for module to host data transfer over the Auxiliary interface is shown in *Figure 22 Module-to-Host Auxiliary Interface Data Transfer*. Flow control between the module and host is achieved through the host only reading the Auxiliary receive data only when it's ready. The module will buffer data as needed. The host can be informed that new data is available from the module, either by polling or via an interrupt. Once the host reads the available data from the receive data register, the module can provide the next sequential data, if any, and set the respective status bits and interrupt as appropriate.

Figure 22 Module-to-Host Auxiliary Interface Data Transfer



An Auxiliary interface host-to-module transaction starts by writing one block at a time in the 0xBC00 address space and setting the appropriate Auxiliary interface host-to-module "Transaction Data Block Ready" flag and the module processes the transaction. Host uses the "Maximum Upgrade Data Block Size" set by the module, and it is the host's responsibility to make sure that each block size is equal to or less than the "Maximum Upgrade Data Block Size". If there is any error in block processing, the host will retransmit the block. It is recommended to force an abort by the host if a CRC error occurs few times on the same block.

Figure 22 Module-to-Host Auxiliary Interface Data Transfer shows the procedure a host would use to read the Auxiliary interface module-to-host transaction data. This transaction bulk data is written a block at a time in the 0xBE00 address space and setting the appropriate Auxiliary interface module-to-host "Transaction Data Block Ready" flag and the host processes each block and updates the status. It is modules responsibility to make sure that each block size equal to or less than the "Maximum Upload Data Block Size". If there is any error in the block processing module will retransmit the block. It is recommended to force an abort by the module if the CRC error occurs few times on the same block. Indication that all module-to-host transaction data has been transferred is conveyed via the data complete status bit. Host sets Maximum Upload Data Block Size.

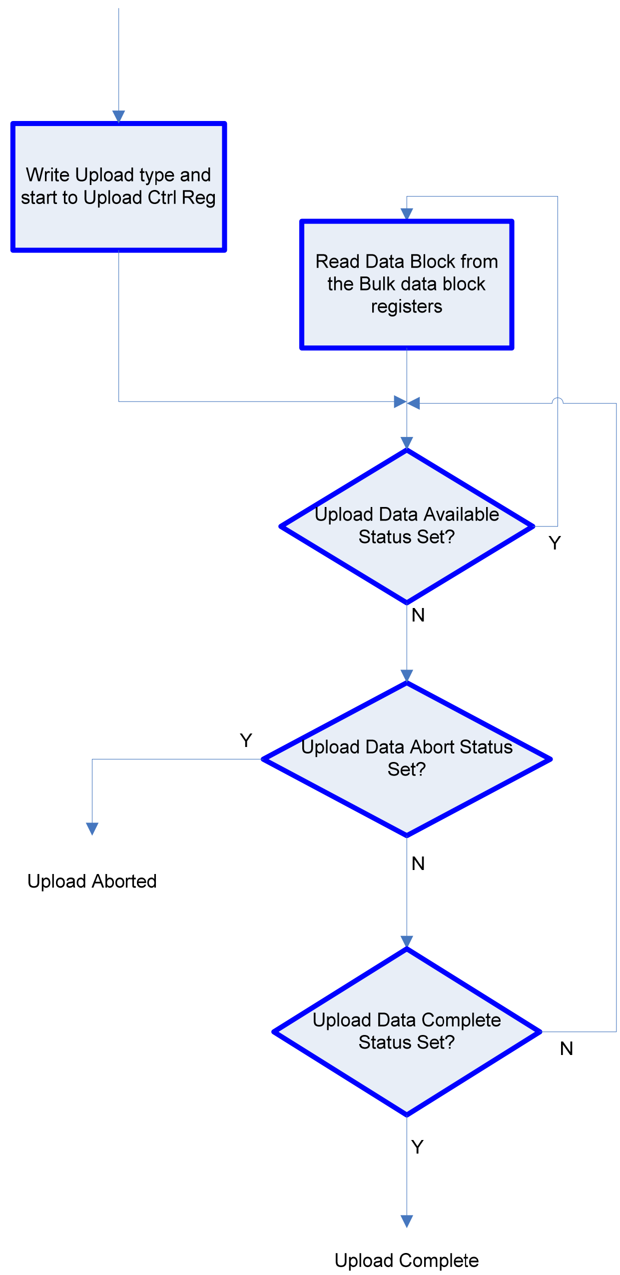
In order to provide maximum flexibility, two Auxiliary interfaces have been defined. This can allow access to two processors at the same time, or to an interactive diagnostic shell and streaming debug output at the same time.

6.2.8 Module-to-Host Generic Data Upload

There may be times when it is advantageous to be able to upload bulk data from the module. This could be for diagnostic purposes for off-line processing or for image recovery. In order to facilitate this, a standard generic mechanism for bulk data upload from the module to the host is defined. Specifying the types of bulk data to upload is outside the scope of the specification, only the low-level transport mechanism is defined in order to assure consistent support across multiple host and module vendors.

Figure 23 Module-to-Host Generic Data Upload shows the procedure a host would use to upload data. The host sets the type of data to upload in the upload type field and requests the upload to start by setting the upload start request bit in the upload control register. The bulk data is written a block at a time in the 0xBE00 address space and setting the "Upload Data Block Ready" flag and the host processes each block and updates the status. It is modules responsibility to make sure that each block size equal to or less than the "Maximum Upload Data Block Size". If there is any error in the block processing module will retransmit the block. It is recommended to force an abort by the module if the CRC error occurs few times on the same block. Indication that all upload data has been transferred is conveyed via the upload data complete status bit. Host sets Maximum Upload Data Block Size.

Figure 23 Module-to-Host Generic Data Upload



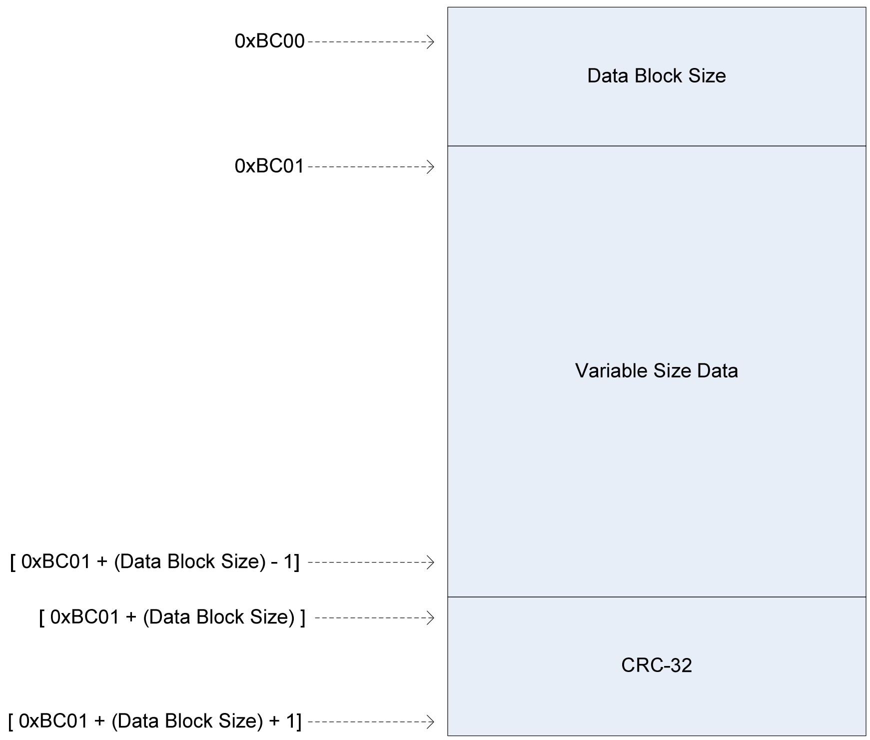
6.2.9 Bulk Data Block Register Structure

6.2.9.1 Host-to-Module Transaction Structure

The Host-to-Module bulk data block starts at register 0xBC00 and can extend up to 0xBDFF. The first register (0xBC00) is Data Block Size (in number of registers for the data portion). The data starts at 0xBC01 followed by the 32-bit CRC as specified in [ITU-T

I.363.5]. For all these registers, MSB stored at low address and LSB stored at high address.

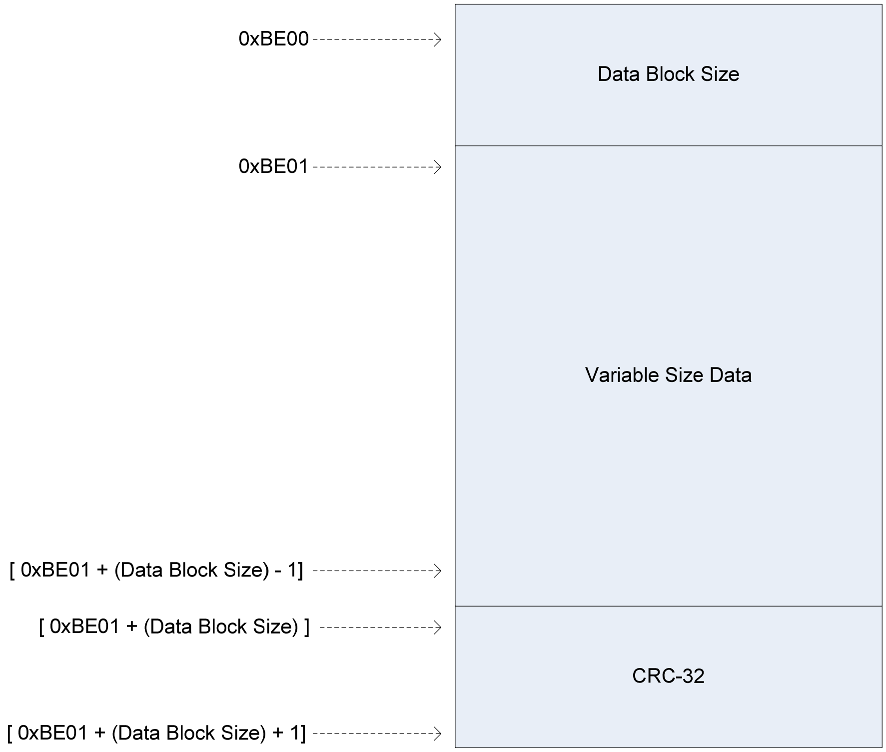
Figure 24 Host-to-Module Bulk Data Block Structure



6.2.9.1 Module-to-Host Transaction Structure

The Module-to-host bulk data block starts at register 0xBE00 and can extend up to 0xBEFF. The first register (0xBE00) is Data Block Size (in number of registers for the data portion). The data starts at 0xBE01 followed by the 32-bit CRC as specified in [ITU-T I.363.5]. For all these registers, MSB stored at low address and LSB stored at high address.

Figure 25 Module-to-Host Bulk Data Block Structure



6.3 MSA-100GLH Module Register Overview

An overview of register modification and additional register allocation required to support the MSA-100GLH Module application beyond the register allocation defined Sections 3 and 5 of this document is given in *Table 36 MSA-100GLH Module Management Register Overview*.

Additional registers are required for:

a) MSA-100GLH Module Control and Digital Diagnostic Monitoring
b) Network TX/RX Lanes
c) Host TX/RX Lanes
d) OTN and FEC Functionality (optional)
e) Modulation dependent functionality (optional-informative)

Table 36 MSA-100GLH Module Management Register Overview

Hex Addr Start	Hex Addr End	Access Type	Allocated Size	Data Bit Width	Description
0000	7FFF	N/A	32768	N/A	Reserved for IEEE 802.3 use.
8000	807F	RO	128	8	CFP NVR 1. Basic ID Registers
8080	80C6	RO	128	8	CFP NVR 2. Extended ID Registers
80C8	80FF				CFP NVR 2. MSA-100GLH Module Alarm/Warning Threshold Registers
8100	817F	RO	128	8	CFP NVR 3. Network Lane BOL Measurement Registers
8180	81FF	RO	128	8	CFP NVR 4. MSA-100GLH Extended ID Registers
8200	83FF	RO	4x128	N/A	MSA Reserved

8400	847F	RO	128	8	Vendor NVR 1. Vendor Data Registers
8480	84FF	RO	128	8	Vendor NVR 2. Vendor Data Registers
8500	87FF	RO	6x128	N/A	MSA Reserved
8800	887F	RW	128	8	User NVR 1. User Data Registers
8880	88FF	RW	128	8	User NVR 2. User Data Registers
8900	8EFF	RO	12x128	N/A	MSA Reserved
8F00	8FFF	N/A	2x128	N/A	Reserved for User private use
9000	9FFF	N/A	4096	N/A	Reserved for Vendor private use
B000	B07F	RW	128	16	MSA-100GLH Module VR1: Command/Setup/Control/FAWS Registers
B080	B17F	RO	2x128	N/A	MSA Reserved
B180	B2FF	RW	3x128	16	MSA-100GLH Module VR1: Network Lane FAWS/Status Registers
B300	B57F	RW	5x128	16	MSA-100GLH Module VR2: Network Lane Control/Data Registers
B580	B5FF	RW	128	16	MSA-100GLH Module VR2: Network Lane OTN/FEC-related Registers (Optional)
B600	B6FF	RW	2x128	16	MSA-100GLH Module VR1: Host Lane FAWS/Control/Status Registers
B700	B77F	RW	2x128	16	MSA-100GLH Module VR1: Host Lane OTN/FEC-related Registers (Optional)
B780	B7FF	RO	128	N/A	MSA Reserved
B800	BAFF	RW	6x128	16	MSA-100GLH Module VR2: Network Lane Modulation Format Dependent Registers (Optional-informative)
BB00	BBFF	RO	2x128	N/A	MSA Reserved
BC00	BFFF	RW	1024	16	MSA-100GLH Module VR2: Bulk Data Transfer Registers

6.4 MSA-100GLH Module Register Description

Detailed descriptions of registers added to the CFP module register set for supporting the MSA-100GLH module management interface are listed in *Table 37 MSA-100GLH Module VR 1 Registers* through *Table 43*. These tables follow the convention and definitions outlined in Section 5, *Table 22*.

The original CFP NVR Tables (Tables 31, 32, 33, and 34 in Version 2.0) for MSA 100GLH have been merged with corresponding tables in section 5 in Version 2.2.

MSA-100GLH Module VR 1

Table 37 MSA-100GLH Module VR 1 Registers lists all registers related to module level command/setup, control and status information and functions necessary to support the MSA-100GLH Module application.

Table 37 MSA-100GLH Module VR 1 Registers

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
Module Command/Setup Registers						
B000 [2.0]	**2**	**WO**	**15~0**	**Password Entry (Optional)**	**Password for module register access control. 2-word value. MSW is in lower address.**	**0000h 0000h**
B002 [2.0]	**2**	**WO**	**15~0**	**Password Change (Optional)**	**New password entry. A 2-word value. MSW is in lower address.**	**0000h 0000h**
B004 [2.0]	**1**			**NVR Access Control**	**User NVRs Restore/Save command. Refer to 4.10.2 for details.**	**0000h**
		RW	15~9	Reserved	**Vendor specific.**	0
		RO	8~6	Reserved		000b
		RW	5	User Restore and Save Command	0: Restore the User NVR section, 1: Save the User NVR section.	0
		RO	4	Reserved		0
		RO	3~2	Command Status	00b: Idle,	00b

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
					01b: Command completed successfully, 10b: Command in progress, 11b: Command failed.	
		RW	1~0	Extended Commands	00b: Vendor specific, 01b: Vendor specific, 10b: Save User Password. If bit 5 = 0, command has no effect. 11b: Restore/Save the User NVRs.	00b
B005 [2.0]	**1**			**PRG_CNTL3 Function Select**	**Selects, and assigns, a control function to PRG_CNTL3.**	**0000h**
		RO	15~8	Reserved		00h
		RW	7~0	Function Select Code	This multi-function input is used as HW_IL_MSB during the Initialize State and it can be programmed to other functions afterward. HW_IL functionality is not applicable to non-pluggable modules, such as OIF MSA-100GLH. 0: No effect, 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL3. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL3 Control (B010h.12) uses an active high logic, that is, 1 = Assert (Reset). 2~127: Reserved - MSA 128~255: Reserved – Vendor-Specific Functions	00h
B006 [2.0]	**1**			**PRG_CNTL2 Function Select**	**Selects, and assigns, a control function to PRG_CNTL2.**	**0000h**
		RO	15~8	Reserved		00h
		RW	7~0	Function Select Code	This multi-function input is used as HW_IL_LSB during the Initialize State and it can be programmed to other functions afterward. HW_IL functionality is not applicable to non-pluggable modules, such as OIF MSA-100GLH. 0: No effect, 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL2. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL2 Control (A010h.11) uses an active high logic, that is, 1 = Assert (Reset). 2~127: Reserved - MSA 128~255: Reserved – Vendor-Specific Functions	00h
B007 [2.0]	**1**			**PRG_CNTL1 Function Select**	**Selects, and assigns, a control function to PRG_CNTL1.**	**0001h**
		RO	15~8	Reserved		00h
		RW	7~0	Function Select Code	0: No effect, 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL1. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL1 Control (A010h.10) uses an active high logic, that is, 1 = Assert (Reset). TRXIC_RSTn is the CFP MSA default function for PRG_CNTL1. 2~127: Reserved - MSA 128~255: Reserved – Vendor-Specific Functions	01h
B008 [2.0]	**1**			**PRG_ALRM3 Source Select**	**Selects, and assigns, an alarm source for PRG_ALRM3.**	**0003h**
		RO	15~8	Reserved		00h
		RW	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON,	03h

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
					2: Ready State, 3: Fault State, MSA default setting, 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, 5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL, 6: RX_NETWORK_LOL, 7: TX_LOSF, 8: TX_HOST_LOL, 9: OOA, Out of alignment, (Only applicable to certain products. If not implemented in the module, Writing 9 to this register has no effect and shall be read as 0. This is also true for Registers B009h and B00Ah). 10: Module Write Ready 11~127: Reserved - MSA 128~255: Reserved – Vendor-Specific Functions	
B009 [2.0]	**1**			**PRG_ALRM2 Source Select**	**Selects, and assigns, an alarm source for PRG_ALRM2.**	**0002h**
		RO	15~8	Reserved		00h
		RW	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON, 2: Ready State, MSA default setting, 3: Fault State, 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, 5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL, 6: RX_NETWORK_LOL, 7: TX_LOSF, 8: TX_HOST_LOL, 9: OOA, Out of alignment, refer to description of B008h for details, 10: Module Write Ready 11~127: Reserved - MSA 128~255: Reserved – Vendor-Specific Functions	02h
B00A [2.0]	**1**			**PRG_ALRM1 Source Select**	**Selects, and assigns, an alarm source for PRG_ALRM1.**	**0001h**
		RO	15~8	Reserved		00h
		RW	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON, MSA default setting, 2: Ready State, 3: Fault State, 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, 5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL, 6: RX_NETWORK_LOL, 7: TX_LOSF, 8: TX_HOST_LOL, 9: OOA, Out of alignment, refer to description of B008h for details, 10: Module Write Ready 11~127: Reserved - MSA 128~255: Reserved – Vendor-Specific Functions	01h
B00B [2.0]	**1**			**Module Operating Control**		**0000h**
		RO	15~14	Reserved		0
		RW	13	RX FEC correction Disable (optional)	0 : RX FEC Correction Enabled 1 : RX FEC Correction Disabled	0b
		RW	12	TX FEC correction Disable (optional)	0 : TX FEC Correction Enabled 1 : TX FEC Correction Disabled	0b
		RW/SC	11	Performance Monitor Tick Synchronization	0: Normal 1: Synchronizes the current one second interval as the start of the multi-second performance monitor data accumulation period specified by the Performance Monitor Interval field	0b

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
		RW	10	Performance Monitor Tick Source	0: Internal 1: External (PM_SYNC Pin)	0b
		RW	9~4	Performance Monitor Interval	Performance monitoring interval 0~63: Represents the number of one second Performance Monitor Tick Intervals plus one for which the Module will accumulate and provide Performance Monitor data. A value of 0 will result in the module providing PM data every 1 second. A value of 9 will result in the module providing PM data every 10 seconds.	00h
		RW	3	Host Interface SFI-S Enable	Used only for 40G operation with legacy SFI-S hosts. 0: Disabled, 1: Enabled	0
		RW	2~0	Module Bi/uni-direction mode Select	000b: Normal bi-directional mode, 001b: Uni-direction TX only mode (optional), 010b: Uni-direction RX only mode (optional), 011b: Special bi-directional mode (optional), 100b~111b: Reserved.	000b
B00C [2.0]	**1**	**RO**	**15~0**	**Command Error Address**	**Address of last command that had an error**	**0000h**
B00D [2.0]	**1**	**RO**	**15~0**	**Command Error Data**	**Command data written of last command that generated an error**	**0000h**
B00E [2.0]	**1**	**RO**	**15~0**	**Command Error Data Mask**	**Mask signifying which bits of command data generated error**	**0000h**
B00F [2.0]	**1**	**RO**		**Command Error Status**	**Provides reason of last command that generated an error**	**0000h**
			15	Out of Range Value	0: No Error, 1: Error	0
			14	Incorrect Value	0: No Error, 1: Error	0
			13	Command Not Valid	0: No Error, 1: Error	0
			12	MDIO Write Done while Module Busy	0: No Error, 1: Error	0
			11	Vendor Specific Error	0: No Error, 1: Error	0
			10~0	Reserved		0
Module Control Registers						
B010 [2.0]	**1**			**Module General Control**		**0000h**
		RW/SC/LH	15	Soft Module Reset	Register bit for module reset function. Writing a 0 to this bit has no effect regardless it was 0 or 1 previously. 1: Module reset assert.	0
		RW	14	Soft Module Low Power	Register bit for module low power function. 1: Assert.	0
		RW	13	Soft TX Disable	Register bit for TX Disable function. 1: Assert.	0
		RW	12	Soft PRG_CNTL3 Control	Register bit for PRG_CNTL3 control function. 1: Assert.	0
		RW	11	Soft PRG_CNTL2 Control	Register bit for PRG_CNTL2 control function. 1: Assert.	0
		RW	10	Soft PRG_CNTL1 Control	Register bit for PRG_CNTL1 control function. 1: Assert.	0
		RW	9	Soft GLB_ALRM Test	Command bit for software forced test signal. When this bit is asserted it generates GLB_ALRM signal. 1: Assert.	0
		RW/SC	8	Processor Reset	Register bit for processor reset function. This bit is self-clearing. Register settings are not affected. This is a Non-Service Affecting reset. 1: Assert.	0
		RO	7~6	Reserved		0
		RO	5	TX_DIS Pin State	Logical state of the TX_DIS pin. 1: Assert.	0
		RO	4	MOD_LOPWR Pin State	Logical state of the MOD_LOPWR pin. 1: Assert.	0
		RO	3	PRG_CNTL3 Pin State	Logical state of the PRG_CNTL3 pin.	0

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
					1: Assert.	
		RO	2	PRG_CNTL2 Pin State	Logical state of the PRG_CNTL2 pin. 1: Assert.	0
		RO	1	PRG_CNTL1 Pin State	Logical state of the PRG_CNTL1 pin. 1: Assert.	0
		RO	0	Reserved		0
B011 [2.0]	**1**			**Network Lane TX Control**	**This control acts upon all the network lanes.**	**0200h**
		RO	15	Reserved		0
		RW	14	TX PRBS Generator Enable	0: Normal operation, 1: PRBS mode. (Optional)	0
		RW	13~12	TX PRBS Pattern	00b:2^7, 01b:2^15, 10b:2^23, 11b:2^31.	00b
		RW	11	TX De-skew Enable	0:Normal, 1:Disable	0
		RW	10	TX FIFO Reset	This bit affects both host and network side TX FIFOs. 0: Normal operation, 1: Reset (Optional).	0
		RW	9	TX FIFO Auto Reset	This bit affects both host and network side TX FIFOs. 0: Not Auto Reset, 1: Auto Reset. (Optional).	1
		RW	8	TX Reset	0: Normal operation, 1: Reset. Definition and implementation are vendor specific.	0
		RW [2.2]	7~5	TX MCLK Control	3-bit field coding the MCLK rate control. **Code / Description / CFP / CFP2/4** 000b / Function disabled 001b / Of network lane rate / Reserved / 1/32 010b / Of network lane rate / 1/8 / 1/8 011b / Of host lane rate / Reserved / Reserved 100b / Of network lane rate / 1/64 / Reserved 101b / Of host lane rate / 1/64 / 1/160 110b / Of network lane rate / 1/16 / Reserved 111b / Of host lane rate / 1/16 / 1/40	000b
		RO	4	Reserved		0b
		RW	3~1	TX Rate Select (10G lane rate)	000b: GbE=10.31, 001b: SDH=9.95, 010b: OTU3=10.7, 011b: OTU4=11.2, 100b: OTU3e1=11.14, 101b: OTU3e2=11.15, 110b~111b: Reserved.	000b
		RW	0	TX Reference CLK Rate Select	0: 1/16, 1: 1/64.	0b
B012 [2.0]	**1**			**Network Lane RX Control**	**This control acts upon all the network lanes.**	**0200h**
		RW	15	Active Decision Voltage and Phase function	This bit activates the active decision voltage and phase function in the module. 0: not active, 1: active. (Optional)	0b
		RW	14	RX PRBS Checker Enable	0: Normal operation, 1: PRBS mode. (Optional)	0b
		RW	13~12	RX PRBS Pattern	00b: 2^7, 01b: 2^15, 10b: 2^23, 11b: 2^31.	00b
		RW	11	RX Lock RX_MCLK to Reference CLK	0: Normal operation, 1: Lock RX_MCLK to REFCLK.	0b
		RW	10	Network Lane Loop-back	0: Normal operation, 1: Network lane loop-back. (Optional)	0b
		RW	9	RX FIFO Auto Reset	0: Not auto reset, 1: Auto reset. (Optional).	1b
		RW	8	RX Reset	0: Normal operation, 1: Reset. Definition and implementation are vendor specific.	0b
		RW [2.2]	7~5	RX MCLK Control (optional)	3-bit field coding the MCLK rate control. **Code / Description / CFP / CFP2/4**	000b

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
					000b; Function disabled	
					001b; Of network lane rate; Reserved; 1/32	
					010b; Of network lane rate; 1/8; 1/8	
					011b; Of host lane rate; Reserved; Reserved	
					100b; Of network lane rate; 1/64; Reserved	
					101b; Of host lane rate; 1/64; 1/160	
					110b; Of network lane rate; 1/16; Reserved	
					111b; Of host lane rate; 1/16; 1/40	
		RW	4	RX FIFO Reset	0: Normal, 1: Reset. (Optional).	0b
		RW	3~1	RX Rate Select	000b: GbE=10.31, 001b:SDH=9.95, 010b:OTU3=10.7, 011b:OTU4=11.2, 100b:OTU3e1=11.14, 101b OTU3e2=11.15, 110b~111b: Reserved.	000b
		RW	0	RX Reference CLK Rate Select	0: 1/16, 1: 1/64.	1b
B013 [2.0]	**1**	**RW**		**Individual Network Lane TX_DIS Control**	**This register acts upon individual network lanes. Note that toggling individual network lane TX disable bit does not change module state.**	**0000h**
			15~0	Lane n Disable	Bits 15~0 disable Lanes 15~0 respectively. 0: Normal, 1: Disable.	0
B014 [2.0]	**1**			**Host Lane Control**	**This control acts upon all the host lanes.**	**0000h**
		RO	15	Reserved		0
		RW	14	TX PRBS Checker Enable	0: Normal operation, 1: PRBS mode. (Optional)	0
		RW	13	TX PRBS Pattern 1	00:2^7, 01:2^15, 10:2^23, 11:2^31.	00b
		RW	12	TX PRBS Pattern 0		
		RO	11	Reserved		0
		RW	10	Host Lane Loop-back Enable	0: Normal operation, 1: Host lane loop-back. (Optional)	0
		RO	9			0
		RO	8	Reserved		0
		RW	7	RX PRBS Generator Enable	0: Normal operation, 1: PRBS mode. (Optional)	0
		RW	6	RX PRBS Pattern 1	00b: 2^7, 01b: 2^15, 10b: 2^23, 11b: 2^31.	00b
		RW	5	RX PRBS Pattern 0		
		RO	4~0	Reserved		0h
B015 [2.2]	**1**			**Module General Control 2**	**This register collects added module general control functions for CFP MSA MIS V2.2**	**0000h**
		RO	15~10	Reserved		0
		RW	9	RX Power Monitor Alarm/Warning Threshold Select	0: MSA default registers 80C0h~80C7h, 1: Host Configured Receive Optical Power Threshold registers B03Ch~B03Fh.	0
		RO	8~0	Reserved		0
Module State Register						
B016 [2.0]	**1**	**RO**		**Module State**	**MSA-100GLH Module state. Only a single bit set at any time.**	**0000h**
			15~9	Reserved		0
			8	High-Power-down State	1: Corresponding state is active. Word value = 0100h.	0
			7	TX-Turn-off State	1: Corresponding state is active. Word value = 0080h.	0
			6	Fault State	1: Corresponding state is active. Word value = 0040h. (Also referred to as MOD_FAULT)	0
			5	Ready State	1: Corresponding state is active. Word value = 0020h. (Also referred to as MOD_READY)	0
			4	TX-Turn-on State	1: Corresponding state is active. Word value = 0010h.	0
			3	TX-Off State	1: Corresponding state is active. Word value = 0008h.	0
			2	High-Power-up State	1: Corresponding state is active. Word value = 0004h.	0

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
			1	Low-Power State	1: Corresponding state is active. Word value = 0002h.	0
			0	Initialize State	1: Corresponding state is active. Word value = 0001h.	0
Module Alarm Summary Registers						
B017	**1**	**RO**		**Network/Host Alarm Status Summary**		
			15	Host TX OTN Status Summary (Optional)	Logical OR of all the enabled bits of Host TX OTN Status Latch register	0
			14	Host TX Alignment Status Summary	Logical OR of all the enabled bits of Host TX Alignment Status Latch register	0
			13	Host RX Alignment Status Summary	Logical OR of all the enabled bits of Host RX Alignment Status Latch register	0
			12	Network RX OTN Status Summary (Optional)	Logical OR of all the enabled bits of Network RX OTN Status Latch register	0
			11	Network RX Alignment Status Summary	Logical OR of all the enabled bits of Network RX Alignment Status Latch register	0
			10	Network TX Alignment Status Summary	Logical OR of all the enabled bits of Network TX Alignment Status Latch register	0
			9~0	Reserved		0
B018 [2.0]	**1**	**RO**		**Global Alarm Summary**		**0000h**
			15	GLB_ALRM Assertion Status	Internal status of global alarm output. 1: Asserted.	0
			14	Host Lane Fault and Status Summary	Logical OR of all the enabled bits of Host Lane Fault and Status Summary register.	0
			13	Network Lane Fault and Status Summary	Logical OR of all the bits in the Network Lane Fault and Status Summary register.	0
			12	Network Lane Alarm and Warning 1 Summary	Logical OR of all the bits in the Network Lane Alarm and Warning 1 Summary register.	0
			11	Module Alarm and Warning 2 Summary	Logical OR of all the enabled bits of Module Alarm and Warning 2 Latch register.	0
			10	Module Alarm and Warning 1 Summary	Logical OR of all the enabled bits of Module Alarm and Warning 1 Latch register.	0
			9	Module Fault Summary	Logical OR of all the enabled bits of Module Fault Status Latch register.	0
			8	Module General Status Summary	Logical OR of all the enabled bits of Module General Status Latch register.	0
			7	Module State Summary	Logical OR of all the enabled bits of Module State Latch register.	0
			6	Network Lane Alarm and Warning 2 Summary	Logical OR of all the enabled bits of Network Lane Alarm and Warning 2 Summary register	0
			5	Network/Host Alarm Status Summary	Logical OR of all the enable bits of Network/Host Alarm Status Summary register.	0
			4	Module Extended Functions Status Summary	Logical OR of all the enabled bits of Module Extended Functions Latch register.	0
			3	Vendor Specific FAWS	Logical OR of all the enabled bits of Vendor Specific FAWS Latch register.	0
			2~1	Reserved		0
			0	Soft GLB_ALRM Test Status	Soft GLB_ALRM Test bit Status.	0
B019 [2.0]	**1**	**RO**		**Network Lane Alarm and Warning 1 Summary**	**Each bit is the logical OR of all enabled bits in each of Network Lane Alarm and Warning 1 Latch registers.**	**0000h**
			15~0	Lane n Alarm and Warning Summary	Logical OR of all enabled bits in Latched Lane n Network Lane Alarm and Warning Register. 1 = Fault asserted. n ranges from 0 to 15.	0
B01A [2.0]	**1**	**RO**		**Network Lane Fault and Status Summary**	**Each bit is the logical OR of all enabled bits in each of the Network Lane fault and Status Latch registers.**	**0000h**
			15~0	Lane n Fault and Status Summary	Logical OR of all enabled bits in Latched Lane n Network Lane Fault and Status Register. 1 = Fault asserted. Lane number n ranges from 0 to 15.	15~0

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
B01B [2.0]	**1**	**RO**		**Host Lane Fault and Status Summary**	**Each bit is the logical OR of all enabled bits in each of the Host Lane fault and Status Latch registers**	**0000h**
			15~0	Lane n Fault and Status Summary	Logical OR of all enabled bits in Latched Lane n Network Lane Fault and Status Register. 1 = Fault asserted. Lane number n ranges from 0 to 15.	0
B01C	**1**	**RO**		**Reserved**		**0**
Module FAWS Registers						
B01D [2.0]	**1**	**RO**		**Module General Status**		**0000h**
			15	Reserved		0
			14	Reserved		0
			13	HW_Interlock	Module internally generated status signal. (FAWS_TYPE_A) 0: If module power <= Host cooling capacity or if hardware Interlock is not used, 1: If module power > Host cooling capacity. For non-pluggable modules (e.g. MSA-100GLH module), PRG_CNTL3 pin should be set to "1" during initialization state.	0
			12~11	Reserved		0
			10	Loss of REFCLK Input	Loss of reference clock input. It is an optional feature. (FAWS_TYPE_B). 0: Normal, 1: Loss of signal.	0
			9	TX_JITTER_PLL_LOL	TX jitter PLL loss of lock. It is an optional feature. (FAWS_TYPE_B). 0: Normal, 1: Loss of lock.	0
			8	TX_CMU_LOL	TX CMU loss of lock. It is the loss of lock indicator on the network side of the CMU. It is an optional feature. (FAWS_TYPE_B). 0: Normal, 1: Loss of lock.	0
			7	TX_LOSF	Transmitter Loss of Signal Functionality. Logic OR of all of Network Lanes TX_LOSF bits. PRG_ALRMx mappable. . (FAWS_TYPE_C, since the TX must be enabled). **Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal.** 0: all transmitter signals functional, 1: any transmitter signal not functional.	0
			6	TX_HOST_LOL	TX IC Lock Indicator. Logic OR of all host lane TX_LOL bits. PRG_ALRMx mappable. (FAWS_TYPE_B). **Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal.** 0: Locked, 1: Loss of lock.	0
			5	RX_LOS	Receiver Loss of Signal. Logic OR of all of network lane RX_LOS bits. (FAWS_TYPE_B). **Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal.** 0: No network lane RX_LOS bit asserted, 1: Any network lane RX_LOS bit asserted.	0
			4	RX_NETWORK_LOL	RX IC Lock Indicator. Logic OR of all network lane RX_LOL bits. PRG_ALRMx mappable. (FAWS_TYPE_B). **Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal.** 0: Locked, 1: Loss of lock.	0
			3	Out of Alignment	Host lane skew out of alignment indicator. Applicable only for some internal implementations. (FAWS_TYPE_B).	0

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
					0: Normal, 1: Out of alignment.	
			2	Performance Monitor Interval Complete	0: Not Done 1:Done.	0
			1	HIPWR_ON	Status bit representing the condition of module in high power status. FAWS Type is not applicable. 0: Module is not in high power on status, 1: Module is in high powered on status.	0
			0	Reserved		0
B01E [2.0]	**1**	**RO**		**Module Fault Status**	**Module Fault Status bit pattern. Only fatal faults that are potentially harmful to the module can trigger the bits here. All the bits are 0: Normal; 1: fault detected. When any bit in this register is a '1', The Module State register will also be set to the Fault State.**	**0000h**
			15	Reserved	Reserved for extension of "other faults" in case of all the bits used up in this register.	0
			14~7	Reserved		0
			6	PLD or Flash Initialization Fault	PLD, CPLD, or FPGA initialization fault. (FAWS_TYPE_A)	0
			5	Power Supply Fault	1: Power supply is out of range. (FAWS_TYPE_A)	0
			4~2	Reserved		000b
			1	CFP Checksum Fault	1: CFP Checksum failed. (FAWS_TYPE_A)	0
			0	Reserved		0
B01F [2.0]	**1**	**RO**		**Module Alarm and Warning 1**		**0000h**
			15~12	Reserved		0000b
			11	Mod Temp High Alarm	Mod temp high Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			10	Mod Temp High Warning	Mod temp high Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			9	Mod Temp Low Warning	Mod temp low Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			8	Mod Temp Low Alarm	Mod temp low Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			7	Mod Vcc High Alarm	Input Vcc high Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			6	Mod Vcc High Warning	Input Vcc high Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			5	Mod Vcc Low Warning	Input Vcc low Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			4	Mod Vcc Low Alarm	Input Vcc low Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			3	Mod SOA Bias High Alarm	SOA bias current high alarm. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
			2	Mod SOA Bias High Warning	SOA bias current high warning. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
			1	Mod SOA Bias Low Warning	SOA bias current low warning. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
			0	Mod SOA Bias Low Alarm	SOA bias current low alarm. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
B020 [2.0]	**1**	**RO**		**Module Alarm and Warning 2**		**0000h**
			15~8	Reserved		0
			7	Mod Aux 1 High Alarm	Module aux ch 1 high alarm. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted..	0
			6	Mod Aux 1 High Warning	Module aux ch 1 high warning. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
			5	Mod Aux 1 Low Warning	Module aux ch 1 low warning. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
			4	Mod Aux 1 Low Alarm	Module aux ch 1 low alarm. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
			3	Mod Aux 2 High Alarm	Module aux ch 2 high alarm. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
			2	Mod Aux 2 High Warning	Module aux ch 2 high warning. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
			1	Mod Aux 2 Low Warning	Module aux ch 2 low warning. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
			0	Mod Aux 2 Low Alarm	Module aux ch 2 low alarm. (FAWS Type is vendor TBD) 0: Normal, 1: Asserted.	0
B021 [2.0]	**1**	**RO**		**Vendor Specific FAWS**	**(Optional) Vendor Specified Module Fault, Alarm, Warning and Status. Contents are specified by the vendor.**	**0000h**
Module FAWS Latch Registers						
B022 [2.0]	**1**			**Module State Latch**		**0000h**
		RO	15~9	Reserved		0
		RO/LH/COR	8	High-Power-down State Latch	1: Latched.	0
		RO/LH/COR	7	TX-Turn-off State Latch	1: Latched.	0
		RO/LH/COR	6	Fault State Latch	1: Latched.	0
		RO/LH/COR	5	Ready State Latch	1: Latched.	0
		RO/LH/COR	4	TX-Turn-on State Latch	1: Latched.	0
		RO/LH/COR	3	TX-Off State Latch	1: Latched.	0
		RO/LH/COR	2	High-Power-up State Latch	1: Latched.	0
		RO/LH/COR	1	Low-Power State Latch	1: Latched.	0
		RO/LH/COR	0	Initialize State Latch	1: Latched.	0
B023 [2.0]	**1**			**Module General Status Latch**		**0000h**
		RO	15	Reserved		0
		RO	14	Reserved		0
		RO/LH/COR	13	HW_Interlock Latch	1: Latched.	0
		RO	12~11	Reserved		0
		RO/LH/COR	10	Loss of REFCLK Input Latch	1: Latched.	0
		RO/LH/COR	9	TX_JITTER_PLL_LOL Latch	1: Latched.	0
		RO/LH/COR	8	TX_CMU_LOL Latch	1: Latched.	0
		RO/LH/COR	7	TX_LOSF Latch	1: Latched. **Note:** Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0
		RO/LH/COR	6	TX_HOST_LOL Latch	1: Latched. **Note:** Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0
		RO/LH/COR	5	RX_LOS Latch	1: Latched. **Note:** Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
		RO/LH/COR	4	RX_NETWORK_LOL Latch	1: Latched. **Note:** Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal.	0
		RO/LH/COR	3	Out of Alignment Latch	1: Latched.	0
		RO/LH/COR	2	Performance Monitor Interval Complete Latch	1: Latched.	0
		RO	1~0	Reserved		000b
B024 [2.0]	**1**			**Module Fault Status Latch**	**Module Fault Status latched bit pattern.**	**0000h**
		RO	15~7	Reserved		0
		RO/LH/COR	6	PLD or Flash Initialization Fault Latch	1: Latched.	0
		RO/LH/COR	5	Power Supply Fault Latch	1: Latched.	0
		RO	4~2	Reserved		000b
		RO/LH/COR	1	CFP Checksum Fault Latch	1: Latched.	0
		RO	0	Reserved		0
B025 [2.0]	**1**			**Module Alarm and Warning 1 Latch**		**0000h**
		RO	15~12	Reserved		0000b
		RO/LH/COR	11	Mod Temp High Alarm Latch	1: Latched.	0
		RO/LH/COR	10	Mod Temp High Warning Latch	1: Latched.	0
		RO/LH/COR	9	Mod Temp Low Warning Latch	1: Latched.	0
		RO/LH/COR	8	Mod Temp Low Alarm Latch	1: Latched.	0
		RO/LH/COR	7	Mod Vcc High Alarm Latch	1: Latched.	0
		RO/LH/COR	6	Mod Vcc High Warning Latch	1: Latched.	0
		RO/LH/COR	5	Mod Vcc Low Warning Latch	1: Latched.	0
		RO/LH/COR	4	Mod Vcc Low Alarm Latch	1: Latched.	0
		RO/LH/COR	3	Mod SOA Bias High Alarm Latch	1: Latched.	0
		RO/LH/COR	2	Mod SOA Bias High Warning Latch	1: Latched.	0
		RO/LH/COR	1	Mod SOA Bias Low Warning Latch	1: Latched.	0
		RO/LH/COR	0	Mod SOA Bias Low Alarm Latch	1: Latched.	0
B026 [2.0]	**1**			**Module Alarm and Warning 2 Latch**		0
		RO	15~8	Reserved		0
		RO/LH/COR	7	Mod Aux 1 High Alarm Latch	1: Latched.	0
		RO/LH/COR	6	Mod Aux 1 High Warning Latch	1: Latched.	0
		RO/LH/COR	5	Mod Aux 1 Low Warning Latch	1: Latched.	0
		RO/LH/COR	4	Mod Aux 1 Low Alarm Latch	1: Latched.	0
		RO/LH/C	3	Mod Aux 2 High Alarm Latch	1: Latched.	0

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
		OR				
		RO/LH/COR	2	Mod Aux 2 High Warning Latch	1: Latched.	0
		RO/LH/COR	1	Mod Aux 2 Low Warning Latch	1: Latched.	0
		RO/LH/COR	0	Mod Aux 2 Low Alarm Latch	1: Latched.	0
B027 [2.0]	**1**	**RO/LH/COR**		**Vendor Specific FAWS Latch**	**(Optional) Vendor Specified Module Fault, Alarm, Warning and Status Latch. Contents are specified by the vendor.**	**0000h**
Module FAWS Enable Registers						
B028 [2.0]	**1**			**Module State Enable**	**GLB_ALRM Enable register for Module State change. One bit for each state.**	**006Ah**
		RO	15~9	Reserved		0
		RW	8	High-Power-down State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	7	TX-Turn-off State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	6	Fault State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	1
		RW	5	Ready State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	1
		RW	4	TX-Turn-on State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	3	TX-Off State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	1
		RW	2	High-Power-up State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	1	Low-Power State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence)	1
		RO	0	Initialize State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
B029 [2.0]	**1**			**Module General Status Enable**	**1: Enable signal to assert GLB_ALRM. Bits 14~0 are AND'ed with corresponding bits in the Module General Status Latch register; the result is used to assert GLB_ALRM. Bit 15 is the master enable of GLB_ALRM and it is AND'ed with the output of the "OR" gate output in Global Alarm Signal Aggregation, Figure 10.**	**A7F8h**
		RW	15	GLB_ALRM Master Enable	1: Enable.	1
		RO	14	Reserved		0
		RW	13	HW_Interlock	1: Enable. For non-pluggable modules (e.g. MSA-100GLH module), this bit is not read.	1
		RO	12~11	Reserved		0
		RW	10	Loss of REFCLK Input Enable	1: Enable.	1
		RW	9	TX_JITTER_PLL_LOL Enable	1: Enable.	1
		RW	8	TX_CMU_LOL Enable	1: Enable.	1
		RW	7	TX_LOSF Enable	1: Enable.	1
		RW	6	TX_HOST_LOL Enable	1: Enable.	1
		RW	5	RX_LOS Enable	1: Enable.	1
		RW	4	RX_NETWORK_LOL Enable	1: Enable.	1
		RW	3	Out of Alignment Enable	1. Enable.	1
		RW	2	Performance Monitor Interval Complete Enable	1. Enable.	1
		RO	1~0	Reserved		000b
B02A [2.0]	**1**			**Module Fault Status Enable**	**These bits are AND'ed with corresponding bits in the Module Fault Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.**	**0062h**

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
		RO	15~7	Reserved		0
		RW	6	PLD or Flash Initialization Fault Enable	1: Enable.	1
		RW	5	Power Supply Fault Enable	1: Enable.	1
		RO	4~2	Reserved		000b
		RW	1	CFP Checksum Fault Enable	1: Enable.	1
		RO	0	Reserved		0
B02B [2.0]	**1**			**Module Alarm and Warning 1 Enable**	**These bits are AND'ed with corresponding bits in the Module Alarm and Warning 1 Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.**	**0FFFh**
		RO	15~12	Reserved		0000b
		RW	11	Mod Temp Hi Alarm Enable	1: Enable.	1
			10	Mod Temp Hi Warn Enable	1: Enable.	1
			9	Mod Temp Low Warning Enable	1: Enable.	1
			8	Mod Temp Low Alarm Enable	1: Enable.	1
			7	Mod Vcc High Alarm Enable	1: Enable.	1
			6	Mod Vcc High Warning Enable	1: Enable.	1
			5	Mod Vcc Low Warning Enable	1: Enable.	1
			4	Mod Vcc Low Alarm Enable	1: Enable.	1
			3	Mod SOA Bias High Alarm Enable	1: Enable.	1
			2	Mod SOA Bias High Warning Enable	1: Enable.	1
			1	Mod SOA Bias Low Warning Enable	1: Enable.	1
			0	Mod SOA Bias Low Alarm Enable	1: Enable.	1
B02C [2.0]	**1**			**Module Alarm and Warning 2 Enable**	**These bits are AND'ed with corresponding bits in the Module Alarm and Warning 2 Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.**	**00FFh**
		RO	15~8	Reserved		00h
		RW	7	Mod Aux 1 High Alarm Enable	1: Enable.	1
			6	Mod Aux 1 High Warning Enable	1: Enable.	1
			5	Mod Aux 1 Low Warning Enable	1: Enable.	1
			4	Mod Aux 1 Low Alarm Enable	1: Enable.	1
			3	Mod Aux 2 High Alarm Enable	1: Enable.	1
			2	Mod Aux 2 High Warning Enable	1: Enable.	1
			1	Mod Aux 2 Low Warning Enable	1: Enable.	1
			0	Mod Aux 2 Low Alarm Enable	1: Enable.	1
B02D [2.0]	**1**	**RW**		**Vendor Specific FAWS Enable**	**(Optional) Vendor Specified Module Fault, Alarm, Warning and Status Enable. Contents are specified by**	**0000h**

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
					the vendor.	
B02E	**1**	**RO**		**Reserved**		**0000h**
Module Analog A/D Value Registers 1						
B02F [2.0]	**1**	**RO**	**15~0**	**Module Temp Monitor A/D Value**	**Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C. Accuracy shall be better than +/- 3 degC over the whole temperature range.**	**0000h**
B030 [2.0]	**1**	**RO**	**15~0**	**Module Power Supply Monitor A/D Value**	**Internally measured transceiver supply voltage, a 16-bit unsigned integer with LSB = 1 mV, yielding a total measurement range of 0 to 65.535 V. Accuracy shall be better than +/- 3% of the nominal value over specified temperature and voltage ranges.**	**0000h**
B031 [2.0]	**1**	**RO**	**15~0**	**SOA Bias Current A/D Value**	**Measured SOA bias current in uA, a 16-bit unsigned integer with LSB = 2 uA, representing a total range of from 0 to 131.072 mA. Accuracy shall be better than +/- 10% of the nominal value over specified temperature and voltage.**	**0000h**
B032 [2.0]	**1**	**RO**	**15~0**	**Module Auxiliary 1 Monitor A/D Value**	**Definition depending upon the designated use.**	**0000h**
B033 [2.0]	**1**	**RO**	**15~0**	**Module Auxiliary 2 Monitor A/D Value**	**Definition depending upon the designated use.**	**0000h**
B034	**4**	**RO**		**Reserved**		**0**
Module PRBS Registers						
B038 [2.0]	**1**	**RO**		**Network Lane PRBS Data Bit Count**	**Network lane data bit counter increments when network lane RX PRBS Checker is enabled. It stops counting when RX PRBS Checker is disabled. It uses an ad-hoc format floating point number with 6-bit unsigned exponent and 10-bit unsigned mantissa.**	**0000h**
			15~10	Exponent	6-bit unsigned exponent.	0
			9~0	Mantissa	10-bit mantissa giving better than 0.1% accuracy in bit counts.	0
B039 [2.0]	**1**			**Host Lane PRBS Data Bit Count**	**Host lane data bit counter increments when host side TX PRBS Checker is enabled. It stops counting when TX PRBS Checker is disabled. It uses an ad-hoc format floating point number with 6-bit unsigned exponent and 10-bit unsigned mantissa.**	**0000h**
		RO	15~10	Exponent	6-bit unsigned exponent	0
		RO	9~0	Mantissa	10-bit mantissa giving better than 0.1% accuracy in bit counts.	0
Module Analog A/D Value Registers 2						
B03A [2.0]	**2**	**RW**	**15~0**	**Real-Time Second Clock**	**Represents number of seconds since Jan. 1, 1970. (MSB at 0xB03Ah, LSB at 0xB03Bh). Write to address B03Ah triggers reading both B03Ah and B03Bh registers**	**0000h**
B03B	**1**	**RO**	**15~0**	**Reserved**		**0**
Host Configured Receive Optical Power Threshold Values						
B03C	**1**	**RW**	**15~0**	**Host Configured Receive Optical Power High Alarm Threshold**	**Valid if the value is between "Host Configured Receive Optical Power High Alarm Permissible Minimum Threshold" (0x80C8-0x80C9) and "Host Configured Receive Optical Power High Alarm Permissible Maximum Threshold" (0x80D0-0x80D1)**	**0**
B03D	**1**	**RW**	**15~0**	**Host Configured Receive Optical Power High Warning Threshold**	**Valid if the value is between "Host Configured Optical Power High Warning Permissible Minimum Threshold" (0x80CA-0x80CB) and "Host Configured Optical Power High Warning Permissible Maximum Threshold" (0x80D2-0x80D3)**	**0**

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
B03E	**1**	**RW**	**15~0**	**Host Configured Receive Optical Power Low Warning Threshold**	**Valid if the value is between "Host Configured Optical Power Low Warning Permissible Minimum Threshold" (0x80CC-0x80CD) and "Host Configured Optical Power Low Warning Permissible Maximum Threshold" (0x80D4-0x80D-0x80D7)**	**0**
B03F	**1**	**RW**	**15~0**	**Host Configured Receive Optical Power Low Alarm Threshold**	**Valid if the value is between "Host Configured Receive Optical Power Low Alarm Permissible Minimum Threshold" (0x80CE-0x80CF) and "Host Configured Receive Optical Power Low Alarm Permissible Maximum Threshold" (0x80D6-0x80D7)**	**0**
Module Extended Functions Control Registers						
B040	**10**	**RO**		**Reserved**		
B04A [2.0]	**1**			**Upload Control**		**0000h**
		RW/SC	15	Upload Start Request	Register bit to request initiation of upload. This bit is self-clearing.	0
		RW	14	Upload Block Processed	1: DONE. 0: NOT DONE.	0
		RW	13	Upload Abort	1: Abort the Upload.	0
		RW	12~11	Upload Block Error Code	0: No Error 1: CRC Image Error 2~7: Reserved.	0
		RO	10~8	Reserved		0
		RW	7~0	Upload Type	Field to specify type of upload data. Values are vendor specific.	0
B04B [2.0]	**1**			**Upload Data**		
		RO	15	Upload Data Block Ready	Set the flag when module completes writing the block to the 0xBC00 address.	0
		RW	14~0	Maximum Upload Data Block Size	Host sets Upload Data Block Size.	1
B04C [2.0]	**1**			**Module Upgrade Data**		
		RW/SC	15	Upgrade Data Block Ready	Set the flag when host completes writing the block to the 0xBC00 address. When cleared by the Module, the Host can then write the next block.	0
		RO	14~0	Maximum Upgrade Data Block Size	Module sets Maximum Upgrade Data Block Size.	1
B04D [2.0]	**1**			**Module Upgrade Control**		
		RW	15~12	Upgrade Command	0: No operation 1: Download Start 2: Download Complete 3: Run Image A 4: Run Image B 5: Abort image download 6: Copy Image A to B 7: Copy Image B to A 8: Commit Image A 9: Commit Image B	
		RO	11~8	MDIO upgrade ready time	During the sw upgrade procedure, after the host issues run image command, the MDIO is not available. MDIO upgrade ready time gives a maximum time for the MDIO to be ready. Value X 5 seconds	0
		RO	7~0	Reserved		0
B04E	**2**	RO		**Reserved**		**0**
Module Extended Functions Status Registers						
B050 [2.0]	**1**	**RO**		**Module Extended Functions Status**		**0000h**
			15	Module Ready for MDIO Write	0: Not Ready, 1: Ready	0
			14	Command Error	0: No Error, 1: Error	0

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
			13	Reserved		0
			12	Auxiliary Interface Instance 1 Rx Data Available (optional)	0: No Data Available, 1: Data Available	0
			11	Auxiliary Interface Instance 2 Rx Data Available (optional)	0: No Data Available, 1: Data Available	0
			10	Auxiliary Interface Instance 1 Rx Data Overflow (optional)	0: No Data Overflow, 1: Data Overflow	0
			9	Auxiliary Interface Instance 2 Rx Data Overflow (optional)	0: No Data Overflow, 1: Data Overflow	0
			8	Upload Data Available	0: No Data Available, 1: Data Available	0
			7	Upload Data Complete	0: Not Done, 1: Done	0
			6~0	Reserved		0
B051 [2.0]	**1**	**RO**		**Module Upgrade Status**		
			15~14	Upgrade Command Status	00: Idle. 01: Command completed successfully. 10: Command in progress. 11: Command failed.	00
			13	Download Image Service Affecting Status	0: Upgrade to Currently Downloaded Image will Not be Service Affecting 1: Upgrade to Currently Downloaded Image will be Service Affecting	0
			12	Image Running	0: Image A 1: Image B	0
			11~10	Image A Status	00: No Image 01: Valid Image Present 10: Image Present is Bad 11: Reserved	0
			9~8	Image B Status	00: No Image 01: Valid Image Present 10: Image Present is Bad 11: Reserved	0
			7	Image Committed	0: Image A 1: Image B	
			6~0	Upgrade Command Failure Reason	0: No Error 1: CRC Image Error 2: Length Image Error 3: Flash Write Error 4: Bad Image Error 5~127: Reserved	0
B052	**2**	**RO**		**Reserved**		**0**
Module Extended Functions Latch Registers						
B054 [2.0]	**1**	**RO/LH/ COR**		**Module Extended Functions Latch**		**0000h**
			15	Module Ready for MDIO Write Latch	0: Not Latched, 1: Latched	0
			14	Command Error Latch	0: Not Latched, 1: Latched	0
			13	Reserved		0
			12	Auxiliary Interface Instance 1 Rx Data Available Latch (optional)	0: Not Latched, 1: Latched	0
			11	Auxiliary Interface Instance 2 Rx Data Available Latch (optional)	0: Not Latched, 1: Latched	0
			10	Auxiliary Interface Instance 1 Rx Data Overflow Latch (optional)	0: Not Latched, 1: Latched	0
			9	Auxiliary Interface Instance 2 Rx Data Overflow Latch	0: Not Latched, 1: Latched	0

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
				(optional)		
			8	Upload Data Available Latch	0: Not Latched, 1: Latched	0
			7	Upload Data Complete Latch	0: Not Latched, 1: Latched	0
			6~0	Reserved		0
B055	**2**	**RO**		**Reserved**		**0**
Module Extended Functions Enable Registers						
B057 [2.0]	**1**	**RW**		**Module Extended Functions Enable**		**0000h**
			15	Module Ready for MDIO Write Enable	0: Disabled, 1: Enabled	0
			14	Command Error Enable	0: Disabled, 1: Enabled	0
			13	Reserved		0
			12	Auxiliary Interface Instance 1 Rx Data Available Enable (optional)	0: Disabled, 1: Enabled	0
			11	Auxiliary Interface Instance 2 Rx Data Available Enable (optional)	0: Disabled, 1: Enabled	0
			10	Auxiliary Interface Instance 1 Rx Data Overflow Enable (optional)	0: Disabled, 1: Enabled	0
			9	Auxiliary Interface Instance 2 Rx Data Overflow Enable (optional)	0: Disabled, 1: Enabled	0
			8	Upload Data Available Enable	0: Disabled, 1: Enabled	0
			7	Upload Data Complete Enable	0: Disabled, 1: Enabled	0
			6~0	Reserved		0
B058	**2**	**RO**		**Reserved**		**0**
Module Extended Functions Data Registers						
B05A [2.0]	**1**			**Host-to-Module Auxiliary Interface Instance 1** (optional)		
		WO	15	Transaction Data Block Ready.	Serial data sent from host to module. Set the flag when host completes writing the block to the 0xBC00 address.	0
		WO	14	Transaction Last Block	1: Last Block in the current transaction. 0: More blocks in the current transaction.	0
		RO	13	Transaction Block Processed	1: DONE 0: NOT DONE.	0
		RO	12	Transaction Abort	1: Abort the transaction.	
		RO	11~10	Transaction Block Error Code	0: No Error 1: CRC Error 2~7: Reserved.	
		RO	9~0	Reserved		0
B05B [2.0]	**1**			**Module-to-Host Auxiliary Interface Instance 1** (optional)		
		RO	15	Transaction Data Block Ready.	Serial data sent from module to host. Set the flag when module completes writing the block to the 0xBE00 address.	0
		RO	14	Transaction Last Block	1: Last Block in the current transaction. 0: More blocks in the current transaction.	0
		WO	13	Transaction Block Processed	1: DONE 0: NOT DONE.	0
		WO	12	Transaction Abort	1: Abort the transaction.	
		WO	11~10	Transaction Block Error	0: No Error	

MSA-100GLH Module VR 1						
Hex Addr.	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
				Code	1: CRC Error 2~7: Reserved.	
		RO	9~0	Reserved		0
B05C [2.0]	**1**			**Host-to-Module Auxiliary Interface Instance 2** (optional)		
		WO	15	Transaction Data Block Ready.	Serial data sent from host to module. Set the flag when host completes writing the block to the 0xBC00 address.	0
		WO	14	Transaction Last Block	1: Last Block in the current transaction. 0: More blocks in the current transaction.	0
		RO	13	Transaction Block Processed	1: DONE 0: NOT DONE.	0
		RO	12	Transaction Abort	1: Abort the transaction.	
		RO	11~10	Transaction Block Error Code	0: No Error 1: CRC Error 2~7: Reserved.	
		RO	9~0	Reserved		0
B05D [2.0]	**1**			**Module-to-Host Auxiliary Interface Instance 2** (optional)		
		RO	15	Transaction Data Block Ready.	Serial data sent from module to host. Set the flag when module completes writing the block to the 0xBE00 address.	0
		RO	14	Transaction Last Block	1: Last Block in the current transaction. 0: More blocks in the current transaction.	0
		WO	13	Transaction Block Processed	1: DONE 0: NOT DONE.	0
		WO	12	Transaction Abort	1: Abort the transaction.	
		WO	11~10	Transaction Block Error Code	0: No Error 1: CRC Error 2~7: Reserved.	
		RO	9~0	Reserved		0
B05E	**34**	**RO**		**Reserved**		**0000h**

6.4.1 MSA-100GLH Module Network Lane Specific Register Tables

Table 38 Network Lane VR 3 (Optional)

Network Lane VR 3						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
Network Lane n Vendor Specific FAWS Registers						
B100 [2.2]	**16**	**RO**		**Network Lane n Vendor Specific FAWS**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
		RO	15	Vendor Specific FAWS bit 15	0: Normal; 1: Asserted.	0
		RO	14~1	Vendor Specific FAWS bit 14~1	0: Normal; 1: Asserted.	0
		RO	0	Vendor Specific FAWS bit 0	0: Normal; 1: Asserted.	0
B110 [2.2]	**16**	**RO**		**Network Lane n Vendor Specific FAWS Latch**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
		RO	15	Vendor Specific FAWS Latch bit 15	0: Normal; 1: Asserted.	0
		RO	14~1	Vendor Specific FAWS Latch bit	0: Normal; 1: Asserted.	0

Network Lane VR 3						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
				14~1		
		RO	0	Vendor Specific FAWS Latch bit 0	0: Normal; 1: Asserted.	0
B120 [2.2]	**16**	RW		**Network Lane n Vendor Specific FAWS Enable**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
			15	Vendor Specific FAWS Enable bit 15	0: Disabled; 1: Enabled.	0
			14~1	Vendor Specific FAWS Enable bit 14~1	0: Disabled; 1: Enabled.	0
			0	Vendor Specific FAWS Enable bit 0	0: Disabled; 1: Enabled.	0
B130	**16**	**RO**	**15~0**	**Reserved**		**0000h**
B140 [2.2]	**16**	**RO**	**15~0**	**Network Lane n Vendor Specific Auxiliary 1 Monitor A/D Value**	**Definition provided by vendor. FAWS mapped to Network Lane n Vendor Specific FAWS bit 15, related to 8090h.**	**0000h**
B150 [2.2]	**16**	**RO**	**15~0**	**Network Lane n Vendor Specific Auxiliary 2 Monitor A/D Value**	**Definition provided by vendor. FAWS mapped to Network Lane n Vendor Specific FAWS bit 14, related to 8098h.**	**0000h**
B160 [2.2]	**16**	**RO**	**15~0**	**Network Lane n Vendor Specific Auxiliary 3 Monitor A/D Value**	**Definition provided by vendor. FAWS mapped to Network Lane n Vendor Specific FAWS bit 13, related to 80A0.**	**0000h**
B170 [2.2]	**16**	**RO**	**15~0**	**Network Lane n Vendor Specific Auxiliary 4 Monitor A/D Value**	**Definition provided by vendor. FAWS mapped to Network Lane n Vendor Specific FAWS bit 12, related to 80A8.**	**0000h**

1 *Table 39 MSA-100GLH Module Network Lane VR 1 Registers*

Network Lane VR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
Network Lane FAWS Registers						
B180 [2.0]	**16**	**RO**		**Network Lane n Alarm and Warning 1**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
			15	Bias High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			14	Bias High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			13	Bias Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			12	Bias Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			11	TX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			10	TX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			9	TX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			8	TX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			7	Laser Temperature High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			6	Laser Temperature High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			5	Laser Temperature Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			4	Laser Temperature Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			3	RX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B) The thresholds for the RX Power High/Low Alarm/Warning are determined by the RX Power Monitor Alarm/Warning Threshold Select in B015h. This comment applies to bits 2~0 as well.	0
			2	RX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			1	RX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			0	RX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0

Network Lane VR 1						
Hex Addr	*Size*	*Access Type*	*Bit*	***Register Name*** *Bit Field Name*	***Description***	*Init Value*
B190 [2.0]	**16**	**RO**		**Network Lane n Alarm and Warning 2**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
			15	Rx Laser Bias Current High Alarm	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			14	Rx Laser Bias Current High Warning	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			13	Rx Laser Bias Current Low Warning	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			12	Rx Laser Bias Current Low Alarm	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			11	Rx Laser Output High Alarm	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			10	Rx Laser Output High Warning	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			9	Rx Laser Output Low Warning	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			8	Rx Laser Output Low Alarm	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			7	Rx Laser Temp High Alarm	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			6	Rx Laser Temp High Warning	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			5	Rx Laser Temp Low Warning	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			4	Rx Laser Temp Low Alarm	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			3	Tx Modulator Bias High Alarm	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			2	Tx Modulator Bias High Warning	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			1	Tx Modulator Bias Low Warning	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
			0	Tx Modulator Bias Low Alarm	0: Normal, 1: Asserted (FAWS_TYPE_B)	0
B1A0 [2.0]	**16**	**RO**		**Network Lane n Fault and Status**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
			15	Lane TEC Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			14	Lane Wavelength Unlocked Fault	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			13	Lane APD Power Supply Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			12~8	Reserved		0
			7	Lane TX_LOSF	0: Normal; 1: Asserted. (PMD) (FAWS_TYPE_C)	0
			6	Lane TX_LOL	0: Normal; 1: Asserted. (Network) (FAWS_TYPE_B)	0
			5	Reserved		0
			4	Lane RX_LOS	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			3	Lane RX_LOL	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			2	Lane RX FIFO error	0: Normal, 1: Error. (FAWS_TYPE_B)	0
			1	Lane RX TEC Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			0	Reserved.		0
Network Lane FAWS Latch Registers						
B1B0 [2.0]	**16**	**RO/LH/ COR**		**Network Lane n Alarm and Warning 1 Latch**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
			15	Bias High Alarm Latch	1: Latched.	0
			14	Bias High Warning Latch	1: Latched.	0
			13	Bias Low Warning Latch	1: Latched.	0
			12	Bias Low Alarm Latch	1: Latched.	0
			11	TX Power High Alarm Latch	1: Latched.	0
			10	TX Power High Warning Latch	1: Latched.	0
			9	TX Power Low Warning Latch	1: Latched.	0
			8	TX Power Low Alarm Latch	1: Latched.	0
			7	Laser Temperature High Alarm Latch	1: Latched.	0
			6	Laser Temperature High Warning Latch	1: Latched.	0
			5	Laser Temperature Low Warning Latch	1: Latched.	0

Network Lane VR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
			4	Laser Temperature Low Alarm Latch	1: Latched.	0
			3	RX Power High Alarm Latch	1: Latched. The thresholds for the RX Power High/Low Alarm/Warning are determined by the RX Power Monitor Alarm/Warning Threshold Select in B015h. This comment applies to bits 2~0 as well.	0
			2	RX Power High Warning Latch	1: Latched.	0
			1	RX Power Low Warning Latch	1: Latched.	0
			0	RX Power Low Alarm Latch	1: Latched.	0
B1C0 [2.0]	**16**	**RO/LH/ COR**		**Network Lane n Alarm and Warning 2 Latch**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
			15	Rx Laser Bias High Alarm Latch	1: Latched	0
			14	Rx Laser Bias High Warning Latch	1: Latched	0
			13	Rx Laser Bias Low Warning Latch	1: Latched	0
			12	Rx Laser Bias Low Alarm Latch	1: Latched	0
			11	Rx Laser Output High Alarm Latch	1: Latched	0
			10	Rx Laser Output High Warning Latch	1: Latched	0
			9	Rx Laser Output Low Warning Latch	1: Latched	0
			8	Rx Laser Output Low Alarm Latch	1: Latched	0
			7	Rx Laser Temp High Alarm Latch	1: Latched	0
			6	Rx Laser Temp High Warning Latch	1: Latched	0
			5	Rx Laser Temp Low Warning Latch	1: Latched	0
			4	Rx Laser Temp Low Alarm Latch	1: Latched	0
			3	Tx Modulator Bias High Alarm Latch	1: Latched	0
			2	Tx Modulator Bias High Warning Latch	1: Latched	0
			1	Tx Modulator Bias Low Warning Latch	1: Latched	0
			0	Tx Modulator Bias Low Alarm Latch	1: Latched	0
B1D0 [2.0]	**16**			**Network Lane n Fault and Status Latch**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
		RO/LH/C OR	15	Lane TEC Fault Latch	1: Latched.	0
		RO/LH/C OR	14	Lane Wavelength Unlocked Fault Latch	1: Latched.	0
		RO/LH/C OR	13	Lane APD Power Supply Fault Latch	1: Latched.	0
		RO	12~8	Reserved		0
		RO/LH/C OR	7	Lane TX_LOSF Latch	1: Latched.	0
		RO/LH/C OR	6	Lane TX_LOL Latch	1: Latched.	0
		RO	5	Reserved		0
		RO/LH/C OR	4	Lane RX_LOS Latch	1: Latched.	0
		RO/LH/C OR	3	Lane RX_LOL Latch	1: Latched.	0
		RO/LH/C	2	Lane RX FIFO Status Latch	1: Latched.	0

Network Lane VR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
		OR				
		RO/LH/COR	1	Lane RX TEC Fault Latch	1: Latched.	0
		RO	0	Reserved		0
Network Lane FAWS Enable Registers						
B1E0 [2.0]	**16**	**RW**		**Network Lane n Alarm and Warning 1 Enable**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**FFFFh**
			15	Bias High Alarm Enable	0: Disable, 1: Enable.	1
			14	Bias High Warning Enable	0: Disable, 1: Enable.	1
			13	Bias Low Warning Enable	0: Disable, 1: Enable.	1
			12	Bias Low Alarm Enable	0: Disable, 1: Enable.	1
			11	TX Power High Alarm Enable	0: Disable, 1: Enable.	1
			10	TX Power High Warning Enable	0: Disable, 1: Enable.	1
			9	TX Power Low Warning Enable	0: Disable, 1: Enable.	1
			8	TX Power Low Alarm Enable	0: Disable, 1: Enable.	1
			7	Laser Temperature High Alarm Enable	0: Disable, 1: Enable.	1
			6	Laser Temperature High Warning Enable	0: Disable, 1: Enable.	1
			5	Laser Temperature Low Warning Enable	0: Disable, 1: Enable.	1
			4	Laser Temperature Low Alarm Enable	0: Disable, 1: Enable.	1
			3	RX Power High Alarm Enable	0: Disable, 1: Enable This comment applies to bits 2~0 as well.. The thresholds for the RX Power High/Low Alarm/Warning are determined by the RX Power Monitor Alarm/Warning Threshold Select in B015h.	1
			2	RX Power High Warning Enable	0: Disable, 1: Enable.	1
			1	RX Power Low Warning Enable	0: Disable, 1: Enable.	1
			0	RX Power Low Alarm Enable	0: Disable, 1: Enable.	1
B1F0 [2.0]	**16**	**RW**		**Network Lane n Alarm and Warning 2 Enable**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**FFFFh**
			15	Rx Laser Bias Current High Alarm Enable	0: Disable, 1: Enable.	1
			14	Rx Laser Bias Current High Warning Enable	0: Disable, 1: Enable.	1
			13	Rx Laser Bias Current Low Warning Enable	0: Disable, 1: Enable.	1
			12	Rx Laser Bias Current Low Alarm Enable	0: Disable, 1: Enable.	1
			11	Rx Laser Output High Alarm Enable	0: Disable, 1: Enable.	1
			10	Rx Laser Output High Warning Enable	0: Disable, 1: Enable.	1
			9	Rx Laser Output Low Warning Enable	0: Disable, 1: Enable.	1
			8	Rx Laser Output Low Alarm Enable	0: Disable, 1: Enable.	1
			7	Rx Laser Temp High Alarm Enable	0: Disable, 1: Enable.	1
			6	Rx Laser Temp High Warning Enable	0: Disable, 1: Enable.	1
			5	Rx Laser Temp Low Warning Enable	0: Disable, 1: Enable.	1
			4	Rx Laser Temp Low Alarm Enable	0: Disable, 1: Enable.	1

Network Lane VR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
			3	Tx Modulator Bias High Alarm Enable	0: Disable, 1: Enable.	1
			2	Tx Modulator Bias High Warning Enable	0: Disable, 1: Enable.	1
			1	Tx Modulator Bias Low Warning Enable	0: Disable, 1: Enable.	1
			0	Tx Modulator Bias Low Alarm Enable	0: Disable, 1: Enable.	1
B200 [2.0]	**16**			**Network Lane n Fault and Status Enable**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**E0D Ch**
		RW	15	Lane TEC Fault Enable	0: Disable, 1: Enable.	1
		RW	14	Lane Wavelength Unlocked Fault Enable	0: Disable, 1: Enable.	1
		RW	13	Lane APD Power Supply Fault Enable	0: Disable, 1: Enable.	1
		RO	12~8	Reserved		0
		RW	7	Lane TX_LOSF Enable	0: Disable, 1: Enable.	1
		RW	6	Lane TX_LOL Enable	0: Disable, 1: Enable.	1
		RO	5	Reserved		0
		RW	4	Lane RX_LOS Enable	0: Disable, 1: Enable.	1
		RW	3	Lane RX_LOL Enable	0: Disable, 1: Enable.	1
		RW	2	Lane RX FIFO Status Enable	0: Disable, 1: Enable.	1
		RW	1	Lane RX TEC Fault Enable	0: Disable, 1: Enable.	1
		RO	0	Reserved		0
Network Lane TX Status Registers						
B210 [2.0]	**16**	**RO**		**Network Lane TX Alignment Status**		
			15	Loss of Alignment	Definition is Module Vendor Specified 0: Not Active, 1: Active	0
			14	Out of Alignment	Definition is Module Vendor Specified 0: Not Active, 1: Active	0
			13	CMU Lock Fault	Definition is Module Vendor Specified 0: Not Active, 1: Active	0
			12	Reference Clock Fault	Definition is Module Vendor Specified 0: Not Active, 1: Active	0
			11	Timing Fault	Definition is Module Vendor Specified 0: Not Active, 1: Active	0
			10~0	Reserved		0
B220 [2.0]	**16**	**RO/LH/ COR**		**Network Lane TX Alignment Status Latch**		
			15	Loss of Alignment Latch	0: Not Latched, 1: Latched	0
			14	Out of Alignment Latch	0: Not Latched, 1: Latched	0
			13	CMU Lock Fault Latch	0: Not Latched, 1: Latched	0
			12	Reference Clock Fault	0: Not Latched, 1: Latched	0
			11	Timing Fault	0: Not Latched, 1: Latched	0
			10~0	Reserved		0
B230 [2.0]	**16**	**RW**		**Network Lane TX Alignment Status Enable**		
			15	Loss of Alignment Enable	0: Disabled, 1: Enabled	0
			14	Out of Alignment Enable	0: Disabled, 1: Enabled	0
			13	CMU Lock Fault Enable	0: Disabled, 1: Enabled	0
			12	Reference Clock Fault	0: Disabled, 1: Enabled	0
			11	Timing Fault	0: Disabled, 1: Enabled	0
			10~0	Reserved		0
B240	**16**	**RO**		**Network Lane TX Alignment**		

Network Lane VR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
[2.0]				**Status PM Interval**		
			15	Loss of Alignment occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			14	Out of Alignment occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			13	CMU Lock Fault occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			12	Reference Clock Fault occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			11	Timing Fault occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			10~0	Reserved		0
Network Lane RX Status Registers						
B250 [2.0]	**16**	**RO**		**Network Lane RX Alignment Status**		
			15	Modem Sync Detect Fault (Optional)	Definition is Module Vendor Specified 0: Not Active, 1: Active	0
			14	Modem Lock Fault (Optional)	Definition is Module Vendor Specified 0: Not Active, 1: Active	0
			13	Loss of Alignment Fault	Definition is Module Vendor Specified 0: Not Active, 1: Active	0
			12	Out of Alignment Fault	Definition is Module Vendor Specified 0: Not Active, 1: Active	0
			11	Timing Fault	Definition is Module Vendor Specified 0: Not Active, 1: Active	0
			10~0	Reserved		0
B260 [2.0]	**16**	**RO/LH/ COR**		**Network Lane RX Alignment Status Latch**		
			15	Modem Sync Detect Fault Latch (Optional)	0: Not Latched, 1: Latched	0
			14	Modem Lock Fault Latch (Optional)	0: Not Latched, 1: Latched	0
			13	Loss of Alignment Fault Latch	0: Not Latched, 1: Latched	0
			12	Out of Alignment Fault Latch	0: Not Latched, 1: Latched	0
			11	Timing Fault Latch	0: Not Latched, 1: Latched	0
			11~0	Reserved		0
B270 [2.0]	**16**	**RW**		**Network Lane RX Alignment Status Enable**		
			15	Modem Sync Detect Fault Enable (Optional)	0: Disabled, 1: Enabled	0
			14	Modem Lock Fault Enable (Optional)	0: Disabled, 1: Enabled	0
			13	Loss of Alignment Enable	0: Disabled, 1: Enabled	0
			12	Out of Alignment Enable	0: Disabled, 1: Enabled	0
			11	Timing Fault Enable	0: Disabled, 1: Enabled	0
			10~0	Reserved		0
B280 [2.0]	**16**	**RO**		**Network Lane RX Alignment Status PM Interval**		
			15	Modem Sync Detect Fault occurred over PM interval (Optional)	0: Did Not Occur, 1: Occurred	0
			14	Modem Lock Fault occurred over PM interval (Optional)	0: Did Not Occur, 1: Occurred	0
			13	Loss of Alignment occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			12	Out of Alignment occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			11	Deskew Lock Fault occurred over PM interval	0: Did Not Occur, 1: Occurred	0

Network Lane VR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
			10	RX LOS occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			9~0	Reserved		0
B290	**112**	**RO**		**Reserved**		0

1 *Table 40 MSA-100GLH Module Network Lane VR 2 Registers*

Network Lane VR 2						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
Network Lane Control 1 Registers						
B300 [2.0]	**16**			**Network Lane n FEC Controls**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
		RW	15~8	Phase Adjustment	This signed 8-bit value represents the phase set point of receive path quantization relative to 0.5 UI, given by: 0.5UI + (Phase Adjustment) / 256 UI. (Optional function) Set this value = -128 (80h) to de-activate this function.	00h
		RW	7~0	Amplitude Adjustment	This signed 8-bit value represents the amplitude threshold of relative amplitude of receive path quantization relative to 50% (Optional function), given by: 50% + (Amplitude Adjustment) / 256 * 100%. (Optional function) Set this value = -128 (80h) to de-activate this function.	00h
B310 [2.0]	**16**	**RO**	**15~0**	**Network Lane n PRBS Rx Error Count**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. This counter increases upon detection of each network lane RX checker error when RX PRBS Checker is enabled. It uses an ad-hoc floating point number format with a 6-bit unsigned exponent and a 10-bit unsigned mantissa. Base of exponent is 2 and Mantissa radix is 0.**	**0000h**
			15~10	Exponent	6-bit unsigned exponent.	0
			9~0	Mantissa	10-bit mantissa giving better than 0.1% accuracy in bit counts.	0
Network Lane A/D Value Measurement Registers						
B320 [2.0]	**16**	**RO**	**15~0**	**Network Lane n TX Laser Bias Current monitor A/D value**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured laser bias current in uA, a 16-bit unsigned integer with LSB = 2 uA, representing a total measurement range of 0 to 131.072 mA. Minimum accuracy shall be +/- 10% of the nominal value over temperature and voltage. This register is for CFP MSA modules.**	**0000h**
B330 [2.0]	**16**	**RO**	**15~0**	**Network Lane n TX Laser Output Power monitor A/D value**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured TX laser output power in dBm,**	**0000h**

Network Lane VR 2						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
					a signed 16-bit integer with LSB = 0.01 dBm. Accuracy must be better than +/- 2 dB over temperature and voltage range. Relative accuracy must be better than 1 dB.	
B340 [2.0]	**16**	**RO**	**15~0**	**Network Lane n TX Laser Temp Monitor A/D value**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** **Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C. Minimum accuracy is +/- 3 degC over temperature range.**	**0000h**
B350 [2.0]	**16**	**RO**	**15~0**	**Network Lane n RX Input Power monitor A/D value**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** **Measured received input power in uW, a 16-bit unsigned integer with LSB = 0.1 uW, representing a power range from 0 to 6.5535 mW (-40 to +8.2 dBm). Value can represent either average received power or OMA depending upon how bit 3 of Register 8080h is set. Accuracy must be better than +/- 2dB over temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss per the appropriate standard. Relative accuracy shall be better than 1 dB over the received power range, temperature range, voltage range, and the life of the product.**	**0000h**
B360 [2.0]	**16**	**RO**	**15~0**	**Network Lane n TX Laser Bias Current monitor A/D value**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** **TX laser bias current monitor in uA, an unsigned 16-bit integer with LSB = 100uA, representing a total measurement range of 0 to 6553.5 mA. Minimum accuracy is +/- 10% of the nominal value over temperature and voltage.**	**0000h**
B370 [2.0]	**16**	**RO**	**15~0**	**Network Lane n RX Laser Bias Current monitor A/D values.**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** **Measured RX laser bias current in uA, an unsigned 16-bit integer with LSB = 100 uA, representing a total measurement range of 0 to 6553.5 mA. Minimum accuracy is +/- 10% of the nominal value over temperature and voltage.**	**0000h**

Network Lane VR 2						
Hex Addr	*Size*	*Access Type*	*Bit*	*Register Name* *Bit Field Name*	*Description*	*Init Value*
B380 [2.0]	**16**	**RO**	**15~0**	**Network Lane n RX Laser Temp Monitor A/D value.**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** **Internally measured temperature in degrees Celsius, a signed 16-bit integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C. Minimum accuracy is +/- 3 degC over t**	**0000h**
B390 [2.0]	**16**	**RO**	**15~0**	**Network Lane n RX Laser Output Power Monitor A/D value**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** **Measured RX laser output power in dBm, a signed 16-bit integer with the LSB = 0.01 dBm**	**0000h**
B3A0 [2.0]	**16**	**RO**	**15~0**	**TX Modulator Bias X/I Monitor A/D value**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** **TX Modulator Bias, a 16-bit unsigned integer with** **LSB = 2mV, yielding a total measurement range of 0 to** **131.072 Volts. Accuracy shall be better than +/-3% of the nominal value over specified operating temperature and voltage range.**	**0**
B3B0 [2.0]	**16**	**RO**	**15~0**	**TX Modulator Bias X/Q Monitor A/D value**		**0**
B3C0 [2.0]	**16**	**RO**	**15~0**	**TX Modulator Bias Y/I Monitor A/D value**		**0**
B3D0 [2.0]	**16**	**RO**	**15~0**	**TX Modulator Bias Y/Q Monitor A/D value**		**0**
B3E0 [2.0]	**16**	**RO**	**15~0**	**TX Modulator Bias X_Phase Monitor A/D value**		**0**
B3F0 [2.0]	**16**	**RO**	**15~0**	**TX Modulator Bias Y_Phase Monitor A/D value**		**0**
Network Lane Control 2 Registers						
B400 [2.0]	**16**			**TX Channel Control**	**Desired TX channel number and grid spacing. 16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0001h**
		RW	15~13	Grid Spacing	000b: 100 GHz grid spacing 001b: 50 GHz grid spacing 010b: 33 GHz grid spacing 011b: 25 GHz grid spacing 100b: 12.5 GHz grid spacing 101b: 6.25 GHz grid spacing 110b ~ 111b: Reserved	000b
		RO	12~10	Reserved		0
		RW	9~0	Channel number	Tx channel number. Channel 0 is an undefined channel number.	001h
B410 [2.0]	**16**	**RW**	**15~0**	**TX Output Power**	**Desired TX output power. 16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** **A signed 16-bit integer with the LSB = 0.01dBm**	**0000h**
B420 [2.0]	**16**			**RX Channel Control**	**Desired RX channel number and grid spacing. 16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0001h**
		RW	15~13	Grid Spacing	000b: 100 GHz grid spacing 001b: 50 GHz grid spacing	000b

Network Lane VR 2						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
					010b: 33 GHz grid spacing 011b: 25 GHz grid spacing 100b: 12.5 GHz grid spacing 101b: 6.25 GHz grid spacing 110b ~ 111b: Reserved	
		RO	13~10	Reserved		0
		RW	9~0	Channel number	Rx channel number. Channel 0 is an undefined channel number.	001h
B430 [2.0]	**16**	**RW**	**15~0**	**TX Fine Tune Frequency (Optional)**	**A signed 16-bit integer with LSB = 1 MHz.**	**000h**
B440 [2.0]	**16**	**RW**	**15~0**	**RX Fine Tune Frequency (Optional)**	**A signed 16-bit integer with LSB = 1 MHz.**	**000h**
B450 [2.0]	**16**	**RO**	**15~0**	**TX Frequency 1**	**Current module TX Frequency 1. An unsigned 16-bit integer with LSB = 1 THz.**	**N/A**
B460 [2.0]	**16**	**RO**	**15~0**	**TX Frequency 2**	**Current module TX Frequency 2. An unsigned 16-bit integer with LSB = 0.05 GHz. Value should not exceed 19999.**	**N/A**
B470 [2.0]	**16**	**RO**	**15~0**	**RX Frequency 1**	**Current module RX Frequency 1. An unsigned 16-bit integer with LSB = 1 THz.**	**N/A**
B480 [2.0]	**16**	**RO**	**15~0**	**RX Frequency 2**	**Current module RX Frequency 2. An unsigned 16-bit integer with LSB = 0.05 GHz. Value should not exceed 19999.**	**N/A**
B490	**16**	**RO**		**Reserved**		**0**
Network Lane TX Performance Monitoring Statistics Registers						
B4A0 [2.0]	**16**	**RO**	**15~0**	**Current Output Power**	**A signed 16-bit integer with the LSB = 0.01 dBm.**	**0000h**
B4B0 [2.0]	**16**	**RO**	**15~0**	**Average Output Power over PM interval**	**A signed 16-bit integer with the LSB = 0.01 dBm.**	**0000h**
B4C0 [2.0]	**16**	**RO**	**15~0**	**Minimum Output Power over PM interval**	**A signed 16-bit integer with the LSB = 0.01 dBm.**	**0000h**
B4D0 [2.0]	**16**	**RO**	**15~0**	**Maximum Output Power over PM interval**	**A signed 16-bit integer with the LSB = 0.01 dBm.**	**0000h**
Network Lane RX Performance Monitoring Statistics Registers						
B4E0 [2.0]	**16**	**RO**	**15~0**	**Current Input Power**	**A signed 16-bit integer with the LSB = 0.01 dBm.**	**0000h**
B4F0 [2.0]	**16**	**RO**	**15~0**	**Average Input Power over PM interval**	**A signed 16-bit integer with the LSB = 0.01 dBm.**	**0000h**
B500 [2.0]	**16**	**RO**	**15~0**	**Minimum Input Power over PM interval**	**A signed 16-bit integer with the LSB = 0.01 dBm.**	**0000h**
B510 [2.0]	**16**	**RO**	**15~0**	**Maximum Input Power over PM interval**	**A signed 16-bit integer with the LSB = 0.01 dBm.**	**0000h**
B520	**96**	**RO**		**Reserved**		**0**
Network Lane OTN/FEC-related Registers (Optional)						
OTN FAWS Registers (Optional)						
B580 [2.0]	**16**	**RO**		**Network Lane RX OTN Status**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	
			15	OTN LOF	0: Not Active, 1: Active	0
			14	OTN OOF	0: Not Active, 1: Active	0
			13	OTN LOM	0: Not Active, 1: Active	0
			12	OTN OOM	0: Not Active, 1: Active	0
			11	OTN IAE	0: Not Active, 1: Active	0
			10	OTN SM BDI	0: Not Active, 1: Active	0
			9	OTN OTU-AIS	0: Not Active, 1: Active	0

Network Lane VR 2						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
			8	OTN ODU-AIS	0: Not Active, 1: Active	0
			7~0	Reserved		0
B590 [2.0]	**16**	**RO/LH/ COR**		**Network Lane RX OTN Status Latch**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	
			15	OTN LOF Latch	0: Not Latched, 1: Latched	0
			14	OTN OOF Latch	0: Not Latched, 1: Latched	0
			13	OTN LOM Latch	0: Not Latched, 1: Latched	0
			12	OTN OOM Latch	0: Not Latched, 1: Latched	0
			11	OTN IAE Latch	0: Not Latched, 1: Latched	0
			10	OTN SM BDI Latch	0: Not Latched, 1: Latched	0
			9	OTN OTU-AIS Latch	0: Not Latched, 1: Latched	0
			8	OTN ODU-AIS Latch	0: Not Latched, 1: Latched	0
			7~0	Reserved		0
B5A0 [2.0]	**16**	**RW**		**Network Lane RX OTN Status Enable**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	
			15	OTN LOF Enable	0: Disabled, 1: Enabled	0
			14	OTN OOF Enable	0: Disabled, 1: Enabled	0
			13	OTN LOM Enable	0: Disabled, 1: Enabled	0
			12	OTN OOM Enable	0: Disabled, 1: Enabled	0
			11	OTN IAE Enable	0: Disabled, 1: Enabled	0
			10	OTN SM BDI Enable	0: Disabled, 1: Enabled	0
			9	OTN OTU-AIS Enable	0: Disabled, 1: Enabled	0
			8	OTN ODU-AIS Enable	0: Disabled, 1: Enabled	0
			7~0	Reserved		0
B5B0 [2.0]	**16**	**RO**		**Network Lane RX OTN Status PM Interval**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	
			15	OTN LOF occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			14	OTN OOF occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			13	OTN LOM occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			12	OTN OOM occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			11	OTN IAE occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			10	OTN SM BDI occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			9	OTN OTU-AIS occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			8	OTN ODU-AIS occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			7~0	Reserved		0
OTN/FEC Network TX Performance Monitoring Registers (Optional)						
B5C0 [2.0]	**1**	**RO/MW**	**15~0**	**FEC Corrected Bits count over PM interval, most significant word**	**Bits 47~32 of 48 bit counter**	**0**
B5C1 [2.0]	**1**	**RO/MW**	**15~0**	**FEC Corrected Bits count over PM interval, middle word**	**Bits 31~16 of 48 bit counter**	**0**
B5C2 [2.0]	**1**	**RO/MW**	**15~0**	**FEC Corrected Bits count over PM interval, least significant word**	**Bits 15~0 of 48 bit counter**	**0**
B5C3 [2.0]	**1**	**RO/MW**	**15~0**	**FEC Uncorrectable Codeword count over PM interval, most significant word**	**Bits 31~16 of 32 bit counter**	**0**
B5C4 [2.0]	**1**	**RO/MW**	**15~0**	**FEC Uncorrectable Codeword count over PM interval, least**	**Bits 15~0 of 32 bit counter**	**0**

Network Lane VR 2						
Hex Addr	*Size*	*Access Type*	*Bit*	*Register Name* *Bit Field Name*	*Description*	*Init Value*
				significant word		
B5C5 [2.0]	**1**	**RO/MW**	**15~0**	**OTN SM BIP-8 error count over PM interval, most significant word**	**Bits 31~16 of 32 bit counter**	**0**
B5C6 [2.0]	**1**	**RO/MW**	**15~0**	**OTN SM BIP-8 error count over PM interval, least significant word**	**Bits 15~0 of 32 bit counter**	**0**
B5C7 [2.0]	**1**	**RO/MW**	**15~0**	**OTN SM BEI count over PM interval, most significant word**	**Bits 31~16 of 32 bit counter**	**0**
B5C8 [2.0]	**1**	**RO/MW**	**15~0**	**OTN SM BEI count over PM interval, least significant word**	**Bits 15~0 of 32 bit counter**	**0**
B5C9	**55**	**RO**		**Reserved**		**0**

6.4.2 MSA-100GLH Module Host Lane Specific Register Tables

Table 41 MSA-100GLH Module Host Lane VR 1 Registers

MSA-100GLH Host Lane VR 1						
Hex Addr	*Size*	*Access Type*	*Bit*	*Register Name* *Bit Field Name*	*Description*	*Init Value*
Host Lane FAWS Status Registers						
B600 [2.0]	**16**			**Host Lane m Fault and Status**	**16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …, M-1. M_max = 16. Actual M is module dependent.**	**0000h**
		RO	15~2	Reserved		0
		RO	1	Lane TX FIFO Error	Lane specific TX FIFO error. (FAWS_TYPE_B) 0: Normal, 1: Error.	0
		RO	0	TX_HOST_LOL	TX IC Lock Indicator, (FAWS_TYPE_B) 0: Locked, 1: Loss of lock.	0
Host Lane FAWS Latch Registers						
B610 [2.0]	**16**			**Host Lane m Fault and Status Latch**	**16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …, M-1. M_max = 16. Actual M is module dependent.**	**0000h**
		RO	15~2	Reserved		0
		RO/LH/COR	1	Lane TX FIFO Error Latch	1: Latched.	0
		RO/LH/COR	0	TX_HOST_LOL Latch	1: Latched.	0
Host Lane FAWS Enable Registers						
B620 [2.0]	**16**			**Host Lane m Fault and Status Enable**	**16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …, M-1. M_max = 16. Actual M is module dependent.**	**0001h**
		RO	15~2	Reserved		0
		RW	1	Lane TX FIFO Error Enable	1: Enable.	0
		RW	0	TX_HOST_LOL Enable	1: Enable.	1
Host Lane Digital PRBS Registers						
B630 [2.0]	**16**	**RO**		**Host Lane m PRBS TX Error Count**	**16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …, M-1. M_max = 16. Actual M is module dependent. This counter increases upon detection of each RX checker error when host lane TX PRBS checker is enabled. It stops**	**0000h**

MSA-100GLH Host Lane VR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
					counting when the TX PRBS checker is disabled. It uses an ad-hoc floating point number format with a 6-bit unsigned exponent and a 10-bit unsigned mantissa.	
			15~10	Exponent	6-bit unsigned exponent.	0
			9~0	Mantissa	10-bit mantissa giving better than 0.1% accuracy in bit counts.	0
Host Lane Control Registers						
B640 [2.0]	**16**			**Host Lane m Control**	**16 registers, one for each host lane, represent 16 host lanes. n = 0, 1, …, M-1. M_max = 16. Actual M is module dependent.**	**0007h**
		RO	15~12	Reserved		
		RW	11~4	Signal Equalization	8 bit field, unsigned integer: 0~127: Reserved - MSA, 128~255: Reserved - Vendor Specific	0
		RW	3~0	Signal Pre/De-emphasis	4-bits unassigned number N represents the pre/de-emphasis applied. Pre/De-emphasis = N * 0.5 dB, N = 0, …, 15. The power on default is 3.5 dB with a value of 7 in this field	7
Host Lane TX Status Registers						
B650 [2.0]	**16**	**RO**		**Host Lane TX Alignment Status**		
			15	CDR Lock Fault	Definition is Module Vendor Specified 0: Not Active, 1: Active	0
			14	Loss of Alignment	Definition is Module Vendor Specified 0: Not Active, 1: Active	0
			13	Out of Alignment	Definition is Module Vendor Specified 0: Not Active, 1: Active	0
			12	Deskew Lock Fault	Definition is Module Vendor Specified 0: Not Active, 1: Active	0
			11~0	Reserved		0
B660 [2.0]	**16**	**RO/LH/ COR**		**Host Lane TX Alignment Status Latch**		
			15	CDR Lock Fault Latch	0: Not Latched, 1: Latched	0
			14	Loss of Alignment Latch	0: Not Latched, 1: Latched	0
			13	Out of Alignment Latch	0: Not Latched, 1: Latched	0
			12	Deskew Lock Fault Latch	0: Not Latched, 1: Latched	0
			11~0	Reserved		0
B670 [2.0]	**16**	**RW**		**Host Lane TX Alignment Status Enable**		
			15	CDR Lock Fault Enable	0: Disabled, 1: Enabled	0
			14	Loss of Alignment Enable	0: Disabled, 1: Enabled	0
			13	Out of Alignment Enable	0: Disabled, 1: Enabled	0
			12	Deskew Lock Fault Enable	0: Disabled, 1: Enabled	0
			11~0	Reserved		0
B680 [2.0]	**16**	**RO**		**Host Lane TX Alignment Status PM Interval**		
			15	CDR Lock Fault occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			14	Loss of Alignment occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			13	Out of Alignment occurred over PM interval	0: Did Not Occur, 1: Occurred	0

MSA-100GLH Host Lane VR 1						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
			12	Deskew Lock Fault occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			11~0	Reserved		0
Host Lane RX Status Registers						
B690 [2.0]	**16**	**RO**		**Host Lane RX Alignment Status**		
			15	Loss of Alignment	Definition is Module Vendor Specified 0: Not Active, 1: Active	0
			14	Out of Alignment	Definition is Module Vendor Specified 0: Not Active, 1: Active	0
			13	CMU Lock Fault	Definition is Module Vendor Specified 0: Not Active, 1: Active	0
			12~0	Reserved		0
B6A0 [2.0]	**16**	**RO/LH/ COR**		**Host Lane RX Alignment Status Latch**		
			15	Loss of Alignment Latch	0: Not Latched, 1: Latched	0
			14	Out of Alignment Latch	0: Not Latched, 1: Latched	0
			13	CMU Lock Fault Latch	0: Not Latched, 1: Latched	0
			12~0	Reserved		0
B6B0 [2.0]	**16**	**RW**		**Host Lane RX Alignment Status Enable**		
			15	Loss of Alignment Enable	0: Disabled, 1: Enabled	0
			14	Out of Alignment Enable	0: Disabled, 1: Enabled	0
			13	CMU Lock Fault Enable	0: Disabled, 1: Enabled	0
			12~0	Reserved		0
B6C0 [2.0]	**16**	**RO**		**Host Lane RX Alignment Status PM Interval**		
			15	Loss of Alignment occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			14	Out of Alignment occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			13	CMU Lock Fault occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			12~0	Reserved		0
B6D0	**48**	**RO**		**Reserved**		**0**
Host Lane OTN/FEC-related Registers (Optional)						
Host Lane OTN FAWS Registers (Optional)						
B700 [2.0]	**16**	**RO**		**Host Lane TX OTN Status**		
			15	OTN LOF	0: Not Active, 1: Active	0
			14	OTN OOF	0: Not Active, 1: Active	0
			13	OTN LOM	0: Not Active, 1: Active	0
			12	OTN OOM	0: Not Active, 1: Active	0
			11	OTN IAE	0: Not Active, 1: Active	0
			10	OTN SM BDI	0: Not Active, 1: Active	0
			9	OTN OTU-AIS	0: Not Active, 1: Active	0
			8	OTN ODU-AIS	0: Not Active, 1: Active	0
			7~0	Reserved		0
B710 [2.0]	**16**	**RO/LH/ COR**		**Host Lane TX OTN Status Latch**		
			15	OTN LOF Latch	0: Not Latched, 1: Latched	0
			14	OTN OOF Latch	0: Not Latched, 1: Latched	0
			13	OTN LOM Latch	0: Not Latched, 1: Latched	0
			12	OTN OOM Latch	0: Not Latched, 1: Latched	0
			11	OTN IAE Latch	0: Not Latched, 1: Latched	0
			10	OTN SM BDI Latch	0: Not Latched, 1: Latched	0
			9	OTN OTU-AIS Latch	0: Not Latched, 1: Latched	0
			8	OTN ODU-AIS Latch	0: Not Latched, 1: Latched	0
			7~0	Reserved		0

MSA-100GLH Host Lane VR 1						
Hex Addr	*Size*	*Access Type*	*Bit*	*Register Name* *Bit Field Name*	*Description*	*Init Value*
B720 [2.0]	**16**	**RW**		**Host Lane TX OTN Status Enable**		
			15	OTN LOF Enable	0: Disabled, 1: Enabled	0
			14	OTN OOF Enable	0: Disabled, 1: Enabled	0
			13	OTN LOM Enable	0: Disabled, 1: Enabled	0
			12	OTN OOM Enable	0: Disabled, 1: Enabled	0
			11	OTN IAE Enable	0: Disabled, 1: Enabled	0
			10	OTN SM BDI Enable	0: Disabled, 1: Enabled	0
			9	OTN OTU-AIS Enable	0: Disabled, 1: Enabled	0
			8	OTN ODU-AIS Enable	0: Disabled, 1: Enabled	0
			7~0	Reserved		0
B730 [2.0]	**16**	**RO**		**Host Lane TX OTN Status PM Interval**		
			15	OTN LOF occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			14	OTN OOF occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			13	OTN LOM occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			12	OTN OOM occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			11	OTN IAE occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			10	OTN SM BDI occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			9	OTN OTU-AIS occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			8	OTN ODU-AIS occurred over PM interval	0: Did Not Occur, 1: Occurred	0
			7~0	Reserved		0
Host Lane OTN/FEC RX Performance Monitoring Registers (Optional)						
B740 [2.0]	**1**	**RO/MW**	**15~0**	**OTN SM BIP-8 error count over PM interval, most significant word (Optional)**	**Bits 31~16 of 32 bit counter**	**0**
B741 [2.0]	**1**	**RO/MW**	**15~0**	**OTN SM BIP-8 error count over PM interval, least significant word (Optional)**	**Bits 15~0 of 32 bit counter**	**0**
B742 [2.0]	**1**	**RO/MW**	**15~0**	**OTN SM BEI count over PM interval, most significant word (Optional)**	**Bits 31~16 of 32 bit counter**	**0**
B743 [2.0]	**1**	**RO/MW**	**15~0**	**OTN SM BEI count over PM interval, least significant word (Optional)**	**Bits 15~0 of 32 bit counter**	**0**
B744	**60**	**RO**		**Reserved**		**0**

6.4.3 MSA-100GLH Network Lane VR2 Registers (Optional)

100G LH DWDM Transmission modulation format dependent performance monitoring statistics registers are specified in *Table 42 MSA-100GLH Network Lane VR 2 Registers*. These registers are optional and their specification is informative.

Table 42 MSA-100GLH Network Lane VR 2 Registers

MSA-100GLH Network Lane VR 2						
Hex Addr	*Size*	*Access Type*	*Bit*	*Register Name* *Bit Field Name*	*Description*	*Init Value*
Network RX Performance Monitoring Statistics Registers (Optional)						
B800 [2.0]	**1**	**RO/MW**	15~0	Current Chromatic Dispersion, most significant word (Optional)	Units are in ps/nm, bits 31~16 of 32 bit counter	0
B810	**1**	**RO/MW**	15~0	Current Chromatic Dispersion, least	Units are in ps/nm, bits 15~0 of 32 bit	0

MSA-100GLH Network Lane VR 2						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
[2.0]				significant word (Optional)	counter	
B820 [2.0]	**1**	**RO/MW**	15~0	Average Chromatic Dispersion over PM interval, most significant word (Optional)	Units are in ps/nm, bits 31~16 of 32 bit counter	0
B830 [2.0]	**1**	**RO/MW**	15~0	Average Chromatic Dispersion over PM interval, least significant word (Optional)	Units are in ps/nm, bits 15~0 of 32 bit counter	0
B840 [2.0]	**1**	**RO/MW**	15~0	Minimum Chromatic Dispersion over PM interval, most significant word (Optional)	Units are in ps/nm, bits 31~16 of 32 bit counter	0
B850 [2.0]	**1**	**RO/MW**	15~0	Minimum Chromatic Dispersion over PM interval, least significant word (Optional)	Units are in ps/nm, bits 15~0 of 32 bit counter	0
B860 [2.0]	**1**	**RO/MW**	15~0	Maximum Chromatic Dispersion over PM interval, most significant word (Optional)	Units are in ps/nm, bits 31~16 of 32 bit counter	0
B870 [2.0]	**1**	**RO/MW**	15~0	Maximum Chromatic Dispersion over PM interval, least significant word (Optional)	Units are in ps/nm, bits 15~0 of 32 bit counter	0
B880 [2.0]	**1**	**RO**	15~0	Current Differential Group Delay (DGD) (Optional)	Units are in ps	0
B890 [2.0]	**1**	**RO**	15~0	Average Differential Group Delay over PM interval (Optional)	Units are in ps	0
B8A0 [2.0]	**1**	**RO**	15~0	Minimum Differential Group Delay over PM interval (Optional)	Units are in ps	0
B8B0 [2.0]	**1**	**RO**	15~0	Maximum Differential Group Delay over PM interval (Optional)	Units are in ps	0
B8C0 [2.0]	**1**	**RO**	15~0	Current SOPMD (Optional)	Definition TBD.	0
B8D0 [2.0]	**1**	**RO**	15~0	Average SOPMD over PM interval (Optional)	Definition TBD.	0
B8E0 [2.0]	**1**	**RO**	15~0	Minimum SOPMD over PM interval (Optional)	Definition TBD.	0
B8F0 [2.0]	**1**	**RO**	15~0	Maximum SOPMD over PM interval (Optional)	Definition TBD.	0
B900 [2.0]	**1**	**RO**	15~0	Current State of Polarization (Optional)	Units are in rad/s	0
B910 [2.0]	**1**	**RO**	15~0	Average State of Polarization over PM interval (Optional)	Units are in rad/s	0
B920 [2.0]	**1**	**RO**	15~0	Minimum State of Polarization over PM interval (Optional)	Units are in rad/s	0
B930 [2.0]	**1**	**RO**	15~0	Maximum State of Polarization over PM interval (Optional)	Units are in rad/s	0
B940 [2.0]	**1**	**RO**	15~0	Current Polarization Dependent Loss (Optional)	Units are in 0.1dB for the LSB	0
B950 [2.0]	**1**	**RO**	15~0	Average Polarization Dependent Loss over PM interval (Optional)	Units are in 0.1dB for the LSB	0
B960 [2.0]	**1**	**RO**	15~0	Minimum Polarization Dependent Loss over PM interval (Optional)	Units are in 0.1dB for the LSB	0
B970 [2.0]	**1**	**RO**	15~0	Maximum Polarization Dependent Loss over PM interval (Optional)	Units are in 0.1dB for the LSB	0
B980 [2.0]	**1**	**RO**	15~0	Current Q (Optional)	Units are in 0.1dB for the LSB	0
B990 [2.0]	**1**	**RO**	15~0	Average Q over PM interval (Optional)	Units are in 0.1dB for the LSB	0
B9A0 [2.0]	**1**	**RO**	15~0	Minimum Q over PM interval (Optional)	Units are in 0.1dB for the LSB	0
B9B0 [2.0]	**1**	**RO**	15~0	Maximum Q over PM interval (Optional)	Units are in 0.1dB for the LSB	0

MSA-100GLH Network Lane VR 2						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
B9C0 [2.0]	**1**	**RO**	15~0	Current Carrier Frequency Offset (Optional)	Units are in MHz	0
B9D0 [2.0]	**1**	**RO**	15~0	Average Carrier Frequency Offset over PM interval (Optional)	Units are in MHz	0
B9E0 [2.0]	**1**	**RO**	15~0	Minimum Carrier Frequency Offset over PM interval (Optional)	Units are in MHz	0
B9F0 [2.0]	**1**	**RO**	15~0	Maximum Carrier Frequency Offset over PM interval (Optional)	Units are in MHz	0
BA00 [2.0]	**1**	**RO**	15~0	Current SNR (Optional)	Units are in 0.1dB for the LSB	0
BA10 [2.0]	**1**	**RO**	15~0	Average SNR over PM interval (Optional)	Units are in 0.1dB for the LSB	0
BA20 [2.0]	**1**	**RO**	15~0	Minimum SNR over PM interval (Optional)	Units are in 0.1dB for the LSB	0
BA30 [2.0]	**1**	**RO**	15~0	Maximum SNR over PM interval (Optional)	Units are in 0.1dB for the LSB	0
BA40	**192**	**RO**		**Reserved**		0

6.4.4 Bulk Data Transfer Segment Registers

Registers 0xBC00h to 0xBFFFh are allocated for bulk data transfer use.

Table 43 Bulk Data Transfer VR 2 Registers

MSA-100GLH Bulk Data Transfer VR 2						
Hex Addr	***Size***	***Access Type***	***Bit***	***Register Name*** *Bit Field Name*	***Description***	***Init Value***
Bulk Data Transfer Registers						
BC00 [2.0]	**512**	**WO**	**15~0**	**Host-To-Module Bulk Data Transfer block**	**Variable size bulk data transfer block for transactions from Host to Module.**	**0**
BE00 [2.0]	**512**	**RO**	**15~0**	**Module-To-Host Bulk Data Transfer block**	**Variable size bulk data transfer block for transactions from Module to Host.**	**0**

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